

UNCLASSIFIED

AD 268 080

*Reproduced
by the*

**ARMED SERVICES TECHNICAL INFORMATION AGENCY
ARLINGTON HALL STATION
ARLINGTON 12, VIRGINIA**



UNCLASSIFIED

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

FILE COPY 268 080

268 080

(Handwritten mark)

TR-951

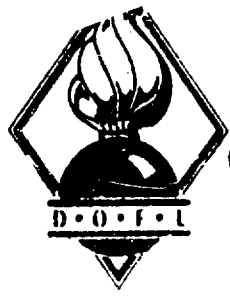
STATUS OF MICROMINIATURIZATION
JUNE 1961

Eleanor F. Horsey
Philip J. Franklin

1 June 1961

ASTIA
DEC 15 1961
(Stamp with vertical text)

258 200



DIAMOND ORDNANCE FUZE LABORATORIES
ORDNANCE CORPS • DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C.

258200

DIAMOND ORDNANCE FUZE LABORATORIES
ORDNANCE CORPS **WASHINGTON 25, D. C.**

DA-5N06-01-010
OMS No. 5210.11.146
OMS No. 5210.11.111
DOFL Proj. No. 90292


TR-951

1 June 1961

STATUS OF MICROMINIATURIZATION -- JUNE 1961

Eleanor F. Horsey and Philip J. Franklin

FOR THE COMMANDER
Approved by



P. A. Guarino
Associate Technical Director



Qualified requesters may obtain copies of this report from ASTIA.

CONTENTS

FOREWORD	4
ABSTRACT	5
1. INTRODUCTION	5
2. MICROMINIATURIZATION BY ASSEMBLY OF PRETESTED CONVENTIONAL OR SPECIALTY COMPONENT PARTS	7
2.1 Hearing-aid-size parts in soldered structures	7
2.2 Hearing-aid-size parts in welded structures	10
2.3 Imitation 2D	10
2.4 Disciplined parts geometry	13
3. PRINTING OR VAPOR DEPOSITION OF MULTI- COMPONENT ASSEMBLIES ON A FLAT INSULATING SUBSTRATE	15
3.1 Original 2D	22
3.2 2D thin-metal-film types	27
3.3 2D multiple-layer thin-metal-film types	35
3.4 Other 2D-related work	37
4. PREPARATION OF COMPLETE CIRCUITS FROM A SOLID BLOCK OF SEMICONDUCTOR MATERIAL	40
4.1 Integrated circuits	40
4.2 Functional circuits	46
5. CONCLUSIONS	50
6. ACKNOWLEDGMENT	50
7. REFERENCES	51

FOREWORD

A prior survey report covering work in electronic microminiaturization up to the date of February 1960 was prepared by these Laboratories and is available from the Office of Technical Services, Department of Commerce, as PB 161 674, N. J. Doctor, "Status of Microminiaturization". In that report it was noted that the field of microminiaturization is moving rapidly and that survey articles on the subject are soon obsolete. It was also stated that, when new techniques were developed, a new survey would be issued.

This present report briefly summarizes past microminiaturization work and describes in greater detail the effort of the past fiscal year. The information given herein is being presented by the second author before the Conference on Components and Materials used in Electronic Engineering, London, England, on 14 June 1961.

ABSTRACT

The status of microminiaturization is summarized under the following three headings: (1) assembly of pretested conventional or specially designed component parts, (2) printing or vapor deposition of multi-component assemblies on flat insulating substrates, and (3) preparation of complete circuits from a solid block of semiconductor material.

Under the first heading, assembly of parts in three-dimensional (3D) soldered structures, in 3D welded structures, in imitation 2D-type structures, and in structures of disciplined geometry is briefly described. The latter structures now include not only the Micro-module but also new pelletized parts.

Under the second heading, the original 2D thin-film type of construction is briefly summarized and then the evolution of this system into experimental circuits containing all thin-film passive parts is shown. The logical next step, preparation of circuits containing thin-film active as well as passive parts, is in even earlier stages of research.

Under the third heading, new developments in integrated and functional circuits are presented. The trend of current work points to the conclusion that equipment available commercially in the next decade will probably take the form of hybrid structures comprising both individually fabricated parts, and single-process parts arrays, all mounted or processed onto an insulating substrate.

1. INTRODUCTION

The term "microminiaturization," as defined by its originator (ref 1) in 1957, is too broad a term to indicate even the maximum size of the electronic designs to be included. Newer related terms, such as microelectronics, micromodules, microcircuitry, and molecular electronics are no better in this respect. Recently, however, authors in the field have begun to define their terms in numbers of component parts per unit volume of the assembly. For example, Brodzinsky et al (ref 2) have defined the term microelectronics to include those electronic circuits and systems whose component parts density is equal to or greater than 2×10^5 equivalent parts per cubic foot. They conceived that a figure of 10^5 was a maximum for the "hearing-aid" (ref 3) type of construction which would, therefore, be eliminated from consideration in microminiaturization discussions. Then, any need of specifying maximum sizes for commercial component parts to be considered microminiature could also be eliminated.

It will be shown later on in this paper that component parts densities of at least 2×10^5 per cubic foot are in fact now being achieved by hearing-aid techniques and, therefore, these techniques may be included in microminiaturization discussions.

For purposes of this paper, the term microminiaturization is defined as the design of electronic circuits and systems having component parts densities greater than 10^5 per cubic foot. For consistency, parts density figures are always reported for a single module because two or more such units, when wired together, give substantial changes in these figures. These decreases are due to the added volumes of interconnections, insulation, and irregularities in the surface of the subassembly.

The principal purposes of this paper are to summarize briefly the various microminiaturization efforts and to describe in greater detail the direction of the effort in the past year. However, a few comments are in order in respect to several advantages claimed for microminiaturized circuits.

The proponents of various microminiaturization techniques have usually claimed at least the following three advantages for their particular miniaturization technique: (1) reduction in size, with consequent reduction in weight, (2) ultimate increased reliability, and (3) ultimate reduced cost by virtue of mass production. It seems timely to state the limitations to each of these proposed advantages.

The reduction in size, and consequent weight, is limited by the required performance of the parts. For example, in order to increase production yields of modules, wider component tolerances are required and these in turn require higher power dissipation. Power dissipation is associated with heat generation and, therefore, thermodynamic considerations actually determine the practical limits of packing densities. Suran (ref 4) notes that "microcircuit fabrication techniques directed to the production of entire circuits or systems in 'monolithic block' structures must face up to tolerance and power problems on a packing density scale so severe that the problems appear to be beyond solution with components made individually by the most sophisticated present-day technologies". He concludes that practical equipment of the foreseeable future will take the form of hybrid structures comprising both individually fabricated components, and single-process component arrays, all mounted or processed onto an insulating substrate.

Claims for ultimate increased reliability are usually based on expected reductions in the number of interconnections as one goes from microminiaturization methods involving assembly of individual components to methods associated with the design of polyfunctional semiconducting materials. Of course, in such a transit, new sources of unreliability, for example, environmental deterioration of a semiconductor surface, may be introduced and thus a net gain in reliability is by no means a certainty. The only case in which it could be stated categorically that microminiaturized equipment is more reliable than its larger counterpart is the case in which the two equipments are exactly the same in every respect except size and weight and in neither case are subject to significant internal overheating. In this case, a tiny structure is more reliable simply because its geometry renders it more resistant to forces due to acceleration, i. e., shock and vibration.

Claims for ultimate reduced cost for microminiaturized circuits can not be substantiated up to the present time. In general, the smaller the circuit, the higher has been its cost. Whether this relationship can be inverted by mass production is questionable. However, it is important to note that in air- and space-craft, where fuel to lift the payload is a part of the cost, microminiaturized systems should be more economical than conventional systems.

The microminiaturization effort will now be summarized under the following three headings: (1) assembly of pretested conventional or specially designed component parts, (2) printing or vapor deposition of multi-component assemblies on flat insulating substrates and (3) preparation of complete circuits from a solid block of semiconductor material.

2. MICROMINIATURIZATION BY ASSEMBLY OF PRETESTED CONVENTIONAL OR SPECIALTY COMPONENT PARTS

The techniques of stacking hearing-aid-size parts on miniature etched wiring boards (ref 3) less than 0.035 inch in thickness, or of assembling similar size parts in welded self-supported structures (ref 5) are by now so well known and widely practiced that another detailed description of these methods and all their variations would serve no useful purpose. Brief analyses of these two techniques are given in Table I where they are compared with two other techniques, one of which has been designated as "Imitation 2D" and the other of which includes both the well-known Micro-module technique, sponsored by the U. S. Army Signal Corps (ref 6), and a newer technique employing pelletized parts.

2.1 Hearing-aid-size parts in soldered structures

Figure 1 is included to illustrate the first-listed technique, namely, a sandwich-type of construction in which hearing-aid-size component parts are hand soldered between printed wiring boards. The device shown (lower left) is a miniature missile-programming timer constructed by Cleveland Metal Specialties Co. according to a design (ref 7) originated by the Diamond Ordnance Fuze Laboratories (DOFL). An enlarged view of one of the basic modules for this device appears in the upper left-hand corner of the figure. This particular module has a component parts density of 3×10^5 /cu. ft. Other modules in this assembly have parts densities as high as 10^6 /cu. ft. The assembly fits into a can 2 x 2 x 3 inches in volume and still leaves space in the can for a mechanical safety and arming mechanism (not shown). By virtue of this miniaturization technique, this electronic timer occupies no more space than the less accurate conventional mechanical timers.

It is probably safe to say that electronic circuits thus miniaturized, and using hand or dip soldering methods, or welding techniques,

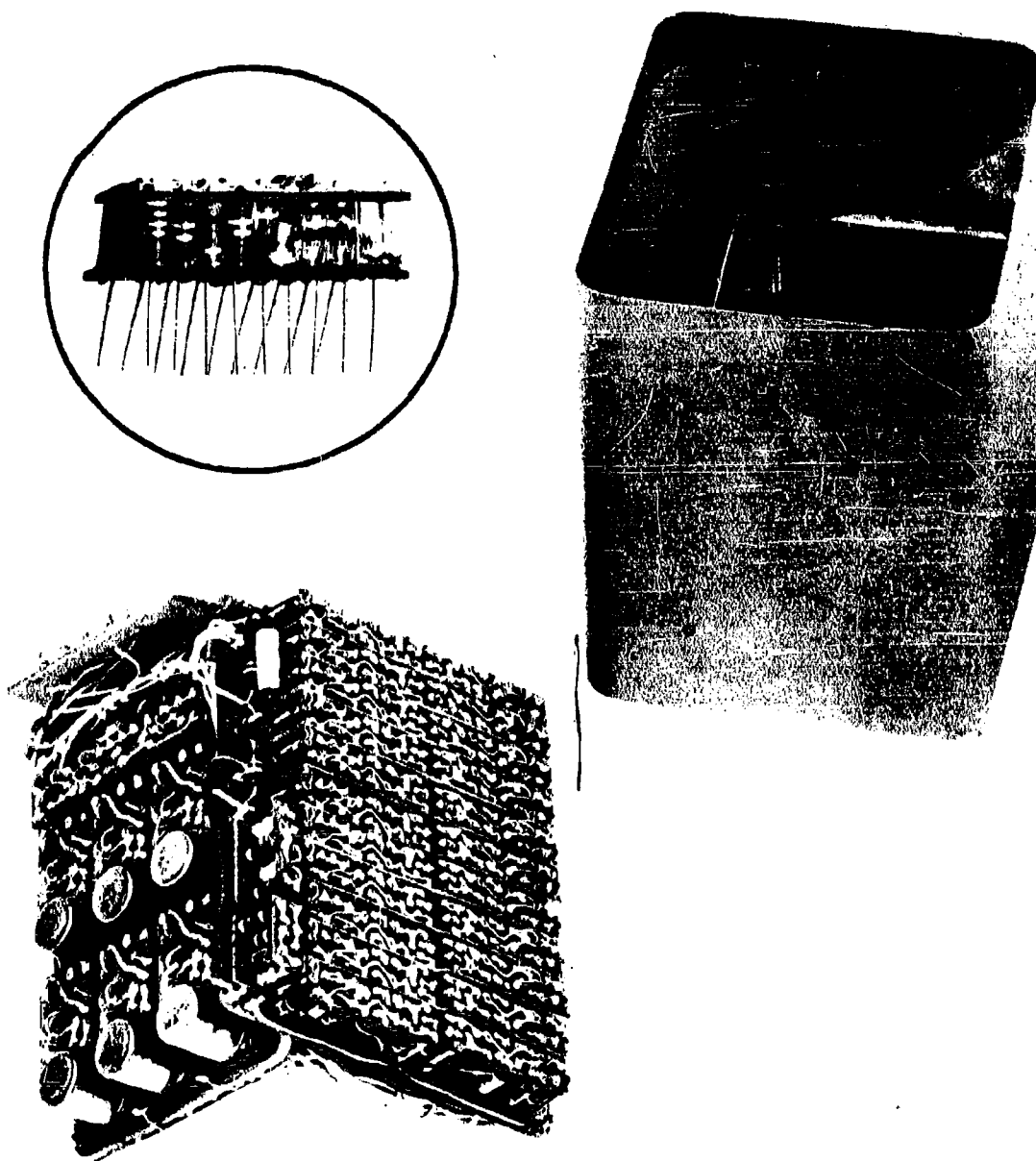
Table 1. Assembly of pretested conventional or specialty component parts, approximate packing density 10^5 to 10^6 parts/in.³.

Identification	Approach	Representative Companies	Features	Problems	Circuits Available	Complexity of Construction	Ease of Interconnection
Hearing-aid-size parts in soldered structure ^{1/}	Parts mounted horizontally or stacked vertically and interconnected by soldering either to wires or to printed wiring boards	Bendix Corp. Burrroughs Corp. Cleveland Metal Specialties Co. Hughes Aircraft Co. Republic Aviation Corp. Waltek Co.	1. Parts all available 2. Maintenance and replacement possible	1. Many solder joints 2. Close soldering may change part-values	Wide range of digital and linear	Very low	Very easy
Hearing-aid-size parts in welded structure ^{2/}	Leads of parts welded to metal ribbons to form self-supporting structures which can be encapsulated	Electronic Engng. Co. Engng. Electronics Co. Francis Associates General Motors Corp. General Electric Co. Raytheon Co. Signican Corp.	1. Parts all available 2. High stiffness-to-weight ratio 3. More reliable and cheaper than soldered packages	1. Special weld cycles required 2. Mechanization difficult 3. Angles make encapsulation difficult	Wide range of digital and linear	Low	Easy
Imitation 2-D	Hearing-aid-size parts placed in cavities in printed circuit boards and soldered to etched copper wiring to resemble a 2D configuration	Cleveland Metal Specialties Co.	1. Parts all available 2. Maintenance and replacement possible	1. Many solder joints 2. Uses many unproven parts	A few digital	Low	Moderate
Disciplined parts geometry ^{3/}	Micro-module: fixed-size parts formed as, in, or on ceramic wafers which are connected to other wafers by means of riser wires soldered to metallized notches in edges of wafers Pelletized parts: fixed-size parts inserted in printed circuit-type substrates	Hughes Aircraft Co. Keystone Carbon Co. King Electronics P. B. Mallory and Co., Inc. Radio Corporation of America	1. Standard geometry	1. Requires revolution in parts industry 2. For micro-module, inflexibility in design 3. For pellets, unproven reliability	Wide range of digital and linear	Moderate	Difficult for micro-module; easy for pelletized components

1/ Trade designations: Dics, Republic Aviation Corp.

2/ Trade designations: Mini Weld, Engng. Electronics Co.; Weld-Paks, Raytheon Co.

3/ Trade designations: Micro-modules, RCA; UCA, P. B. Mallory and Co., Inc.; Dot Components, Hughes Aircraft Co.



694-61

Figure 1. Missile-programming timer (Cleveland Metal Specialties Co.) constructed with hearing-aid-size parts in a soldered structure.

are being produced by practically every electronic company because the armed forces cannot wait for equipment miniaturized by the more complicated techniques.

2.2 Hearing-aid-size parts in welded structures

In Figure 2, a welded assembly made by The Sippican Corp. is shown. The device is a pulse clock from the Polaris FBM Guidance Computer. In this photograph the point-to-point welding has been finished but the "matrix" has not yet been welded to the side of the stick. The general construction procedure (ref 8) follows.

Component parts are first stacked like cordwood, placed upright with their leads protruding through two suitably punched Mylar tapes which serve only for support, and then their leads are welded to nickel ribbons to form groups of subcircuits. Two strips of suitably punched Mylar tape are placed over the wiring for insulation, and then two more suitably punched Mylar tapes, each containing a grid or matrix of nickel wires, are added. These wires are welded at appropriate locations to component leads to form a complete module which is then encapsulated.

Welding techniques were first applied by Francis Associates [under contract to the MIT Instrumentation Laboratories (ref 5)]. Now the Sippican Corp., Francis Associates, and Electronic Engineering Co. are affiliated with Engineered Electronics Co. in the production and sale of systems called "MiniWeld" which employ welded modules of the above-described type. Parts densities greater than 10^5 per cubic foot have been readily achieved with hearing-aid-size components, and the circuits are claimed to be more reliable than soldered ones because: (1) solder flux is eliminated and (2) connections can be made closer to the body of the component without damaging it, thereby resulting in tighter packing and higher stiffness for the same weight.

In 1959, a committee was formed to attempt to set military specifications for welded circuitry and to act as a body in requesting from component parts manufacturers such items as parts with easily weldable rather than easily solderable leads. More than thirty companies are now represented in this committee.

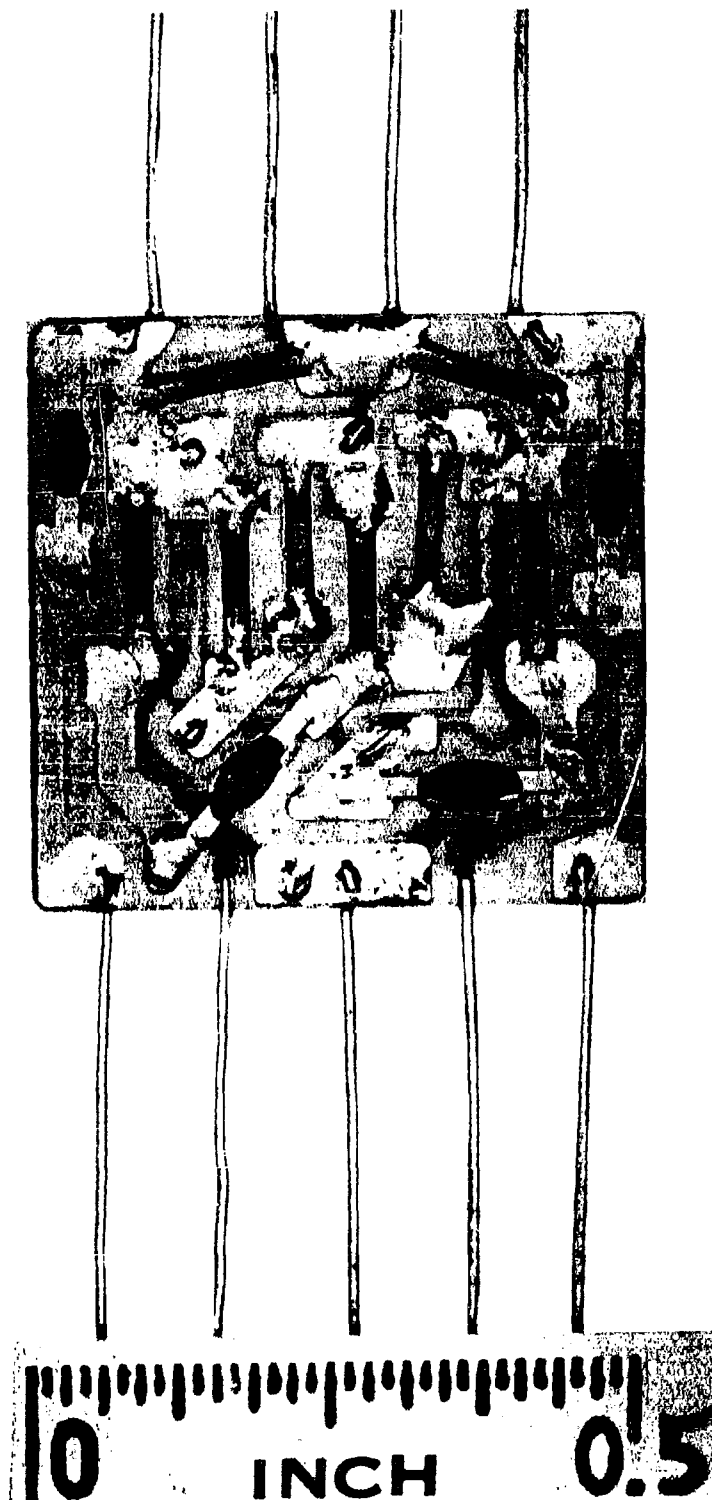
2.3 Imitation 2D

An "imitation 2-D" circuit is shown in Figure 3. This 0.5 x 0.5 x 0.035-inch circuit was constructed by Cleveland Metal Specialties Co. which originated this technique.

Imitation 2-D circuits have not been widely described in the literature. Recently they were included in a discussion (ref 9) of the original 2-D circuits (ref 10) even though they are not even of the same type. Thus it is worthwhile to emphasize that these imitation



Figure 2. Pulse clock (The Sippican Corp.) constructed with hearing-aid-size parts in a welded structure.



695-61

Figure 3. Binary divider (Cleveland Metal Specialties Co.) constructed with hearing-aid-size parts inserted in an etched circuit board (Imitation 2D).

2D circuits employ not a single deposited component part but only commercially available parts. However, since these parts are inserted in cavities in printed circuit boards, the configuration of the finished circuit looks very similar to that of the original 2D circuits, and component parts densities of the same order of magnitude (10^6 /cu. ft.) have been achieved.

Imitation 2D techniques, as well as sandwich techniques, are being utilized by a group of firms engaged in the MICRAM program (Microminiature Individual Component Reliable Assembled Modules). Cleveland Metal Specialties Co. is coordinating this program.

2.4 Disciplined parts geometry

The disciplined-parts-geometry approach, as originally applied by Radio Corporation of America (ref 11) as prime contractor for the Army Signal Corps, consisted essentially in stacking single-component uniformly shaped wafers, or microelements, and interconnecting them by means of riser wires attached around the periphery of the stack. An exploded view of a typical Micro-module of the period 1957-59 is shown in Figure 4. For purposes of the classification within this present paper, it is important to note that none of these micro-elements consists of multi-component parts on a single wafer. Instead, they consist of a single part on a single wafer, or at most, multiples of the same type of part on a single wafer. Some micro-elements of the present period employ as many as two component parts on a wafer, for example, a multi-layer ceramic capacitor with a deposited thin metallic film resistor, or a ferrite core inductor mounted on a ceramic capacitor.

Because of concurrent developments of multi-component circuits, and of integrated and functional circuits, current thinking (ref 12) in the Micro-module program recognizes the immediate volume savings to be made by placing many different component parts on a single wafer, and the eventual savings to be made by placing polyfunctional circuits on a single wafer. When this is done, the Micro-module will be reclassifiable as another multi-component, integrated, or functional circuit.

From the above discussion, it is apparent that the principal contribution of the Micro-module program up to the present is its packaging scheme and, further, that this packaging scheme is superior to any of the others illustrated thus far in this discussion for the simple reason that it most readily permits automation in the production of the final circuit or system. At present, each wafer is 0.310 inch square, ca. 0.010 inch thick, and has on each edge three uniformly sized and spaced notches for lead attachment. Notches are metallized, riser wires are soldered to selected notches, at least six risers are connected to terminal pins for rigidity, and the stack is potted. A 0.010-inch gap is allowed between each wafer. The general scheme is a scaled down

TYPICAL WAFER COMPONENTS

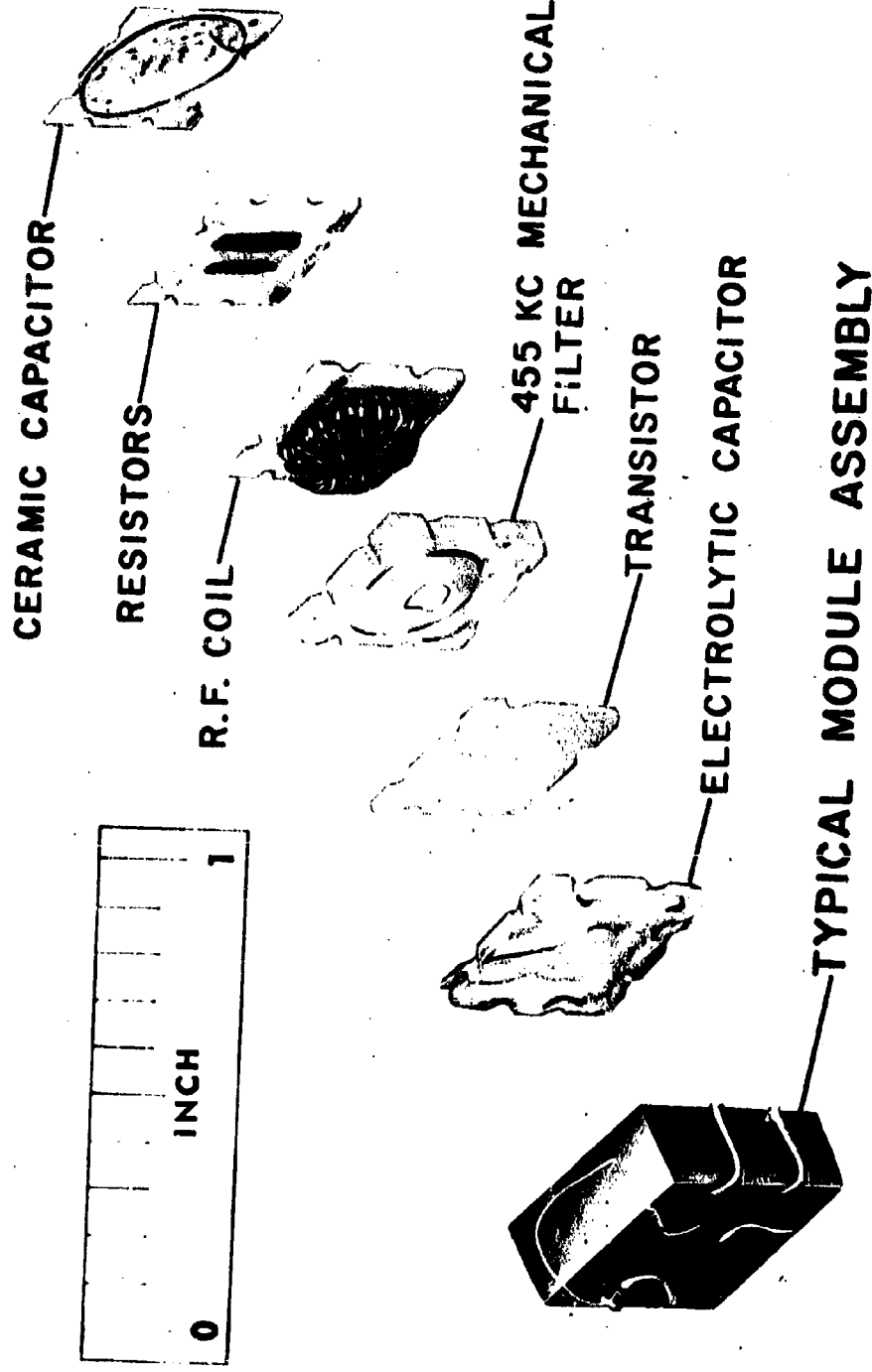


Figure 4. Exploded view of Micro-module (Army Signal Corps - RCA) constructed with a variable number of single or multi-element wafers of fixed geometry.

version of that employed earlier in the non-miniature project, Tinkertoy (ref 13). As presently practiced, however, the scheme requires a major revolution in the electronic parts industry yet offers little or no size reduction over that which can be obtained with commercially available hearing-aid-size parts. Frequency limitations also arise from the inductances of the riser wires.

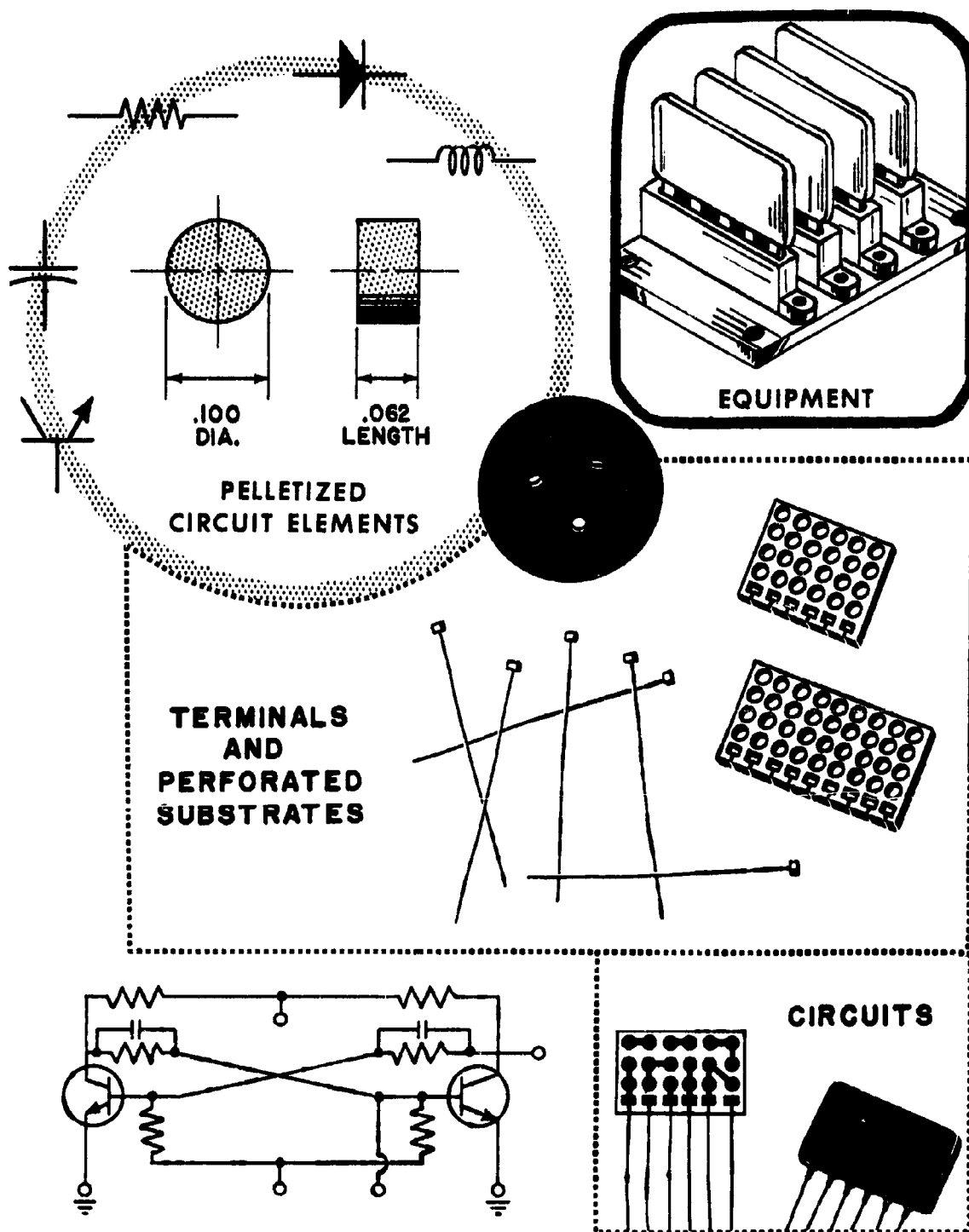
Within the past year, another attempt at a disciplined parts geometry has been made in the form of pelletized components (ref 14 and 15). Mallory's pelletized parts, which thus far are limited to passive elements, are planned to be 0.030 or 0.063 inch in thickness and 0.100 or 0.250 inch in diameter. These pellets are first inserted in holes in a printed circuit board, are then connected to the pattern by means of conductive cement, and finally are encapsulated in epoxy resin (see Fig. 5). Hughes' pelletized active elements are slightly smaller than Mallory's passive elements, and are sometimes plugged into plated-through holes in circuit boards made of epoxy-glass (see Fig. 6), or into Fotoform housings (see Fig. 7). It is recognized that these structures are well suited to the eventual packaging of complete circuits.

Pelletized parts permit component parts densities greater than 10^5 /cu. ft., about the same order of magnitude as that possible with the Micro-module. Like the Micro-module elements, these pelletized parts require a major revolution in the parts manufacturing industry, but they permit significantly easier interconnections and a significantly reduced number of solder joints. For these reasons they will probably find many industrial applications.

Up to this point, commercial parts available for use in micro-miniaturized equipment have been referred to only as a group and the majority of survey articles on this subject are no more specific. For this reason an effort has been made to compile a representative list of suitable component parts and this list appears in Table II. It includes not only conventional small component parts but also new and more exotic parts such as the pelletized parts described above, and thin-film parts to be discussed in the next section. In Figure 8 there are shown some commercially available connectors suitable for use in microminiaturized assemblies.

3. PRINTING OR VAPOR DEPOSITION OF MULTI-COMPONENT ASSEMBLIES ON A FLAT INSULATING SUBSTRATE

The miniaturization methods to be summarized in this section (see Table III) all fall in the general category of two-dimensional (2-D) in the sense that all employ printed or otherwise deposited thin-film passive components whose thickness is practically negligible when compared with area, and all employ a variety of component parts on a single substrate. Thus far, active elements are generally inserted in cavities in the substrate.



697-81

Figure 5. Microminiaturized equipment (P. R. Mallory and Co., Inc.) constructed with a variable number of pelletized component parts of fixed geometry.

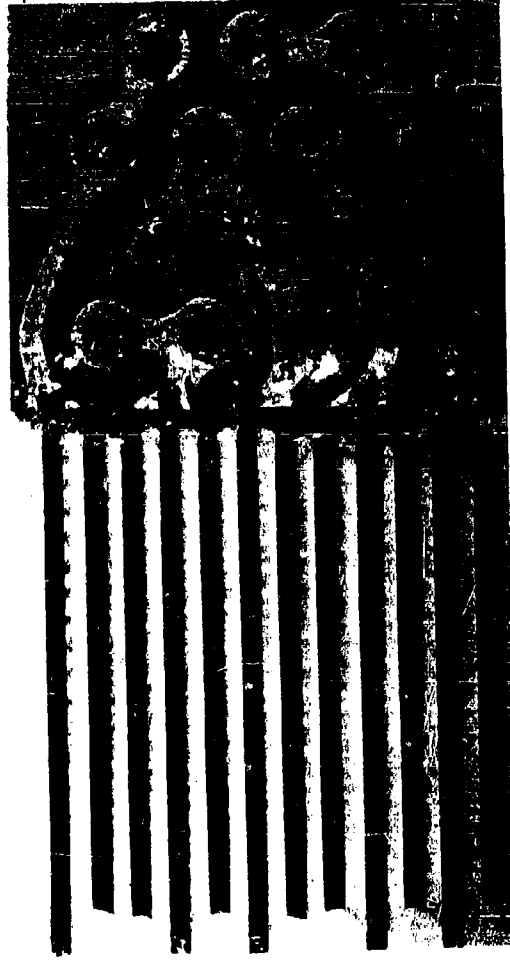
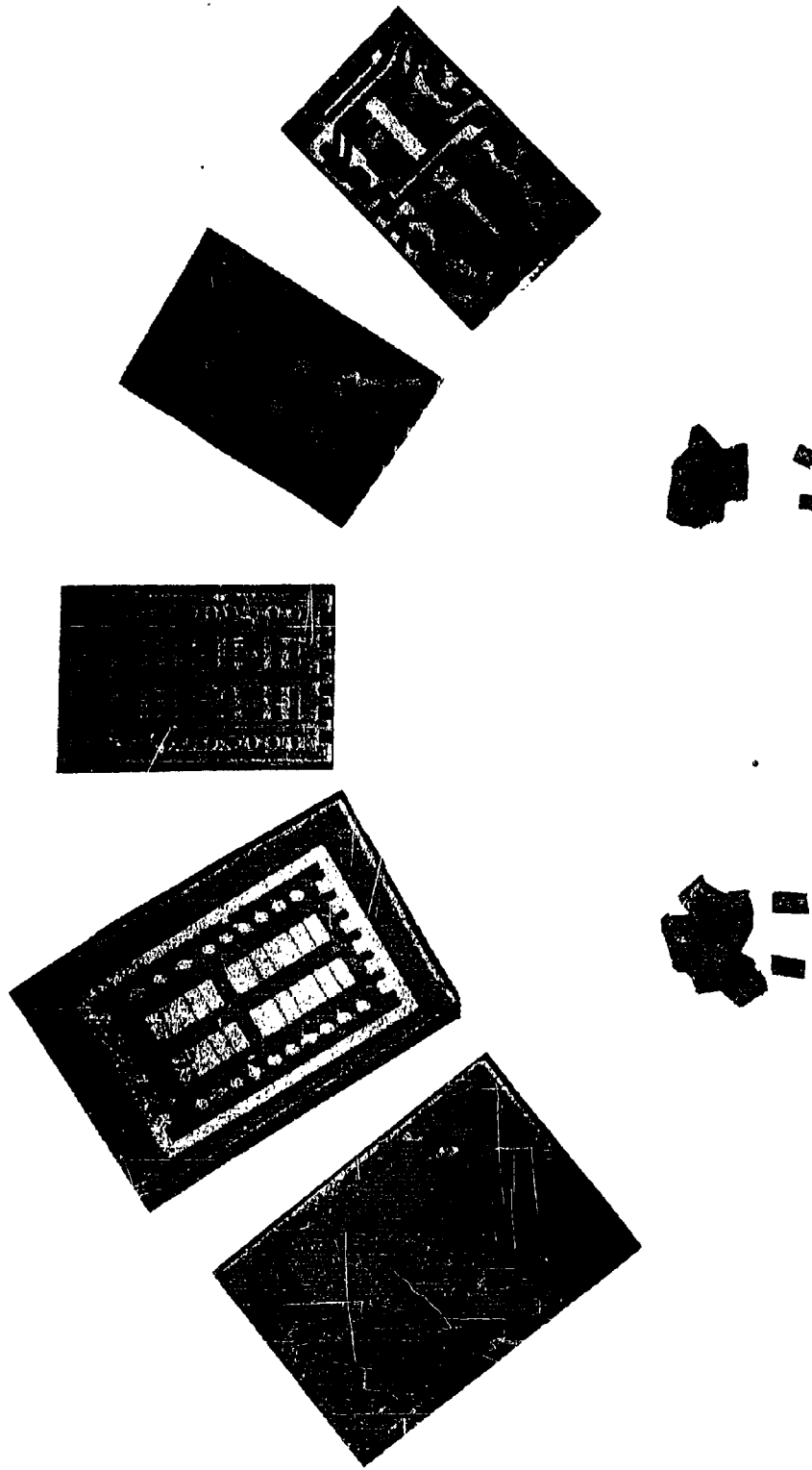


Figure 6. Micro-rectifier network (Hughes Aircraft Co.) employs pelletized diodes and resistors inserted in an epoxy-glass circuit board which is connected to a printed cable.



699-61

Figure 7. Corning Glass Works' steps in preparation of Fotoceram substrates which are perforated to receive pelletized component parts in Fotoform housings: background, (1) photosensitive glass, (2) same after u-v application, and heat development, of pattern image, (3) after acid etching, (4) after heat conversion to crystalline ceramic, (5) after application of metallizing pattern; foreground, left, housings for capacitors and, right, housings for diodes.

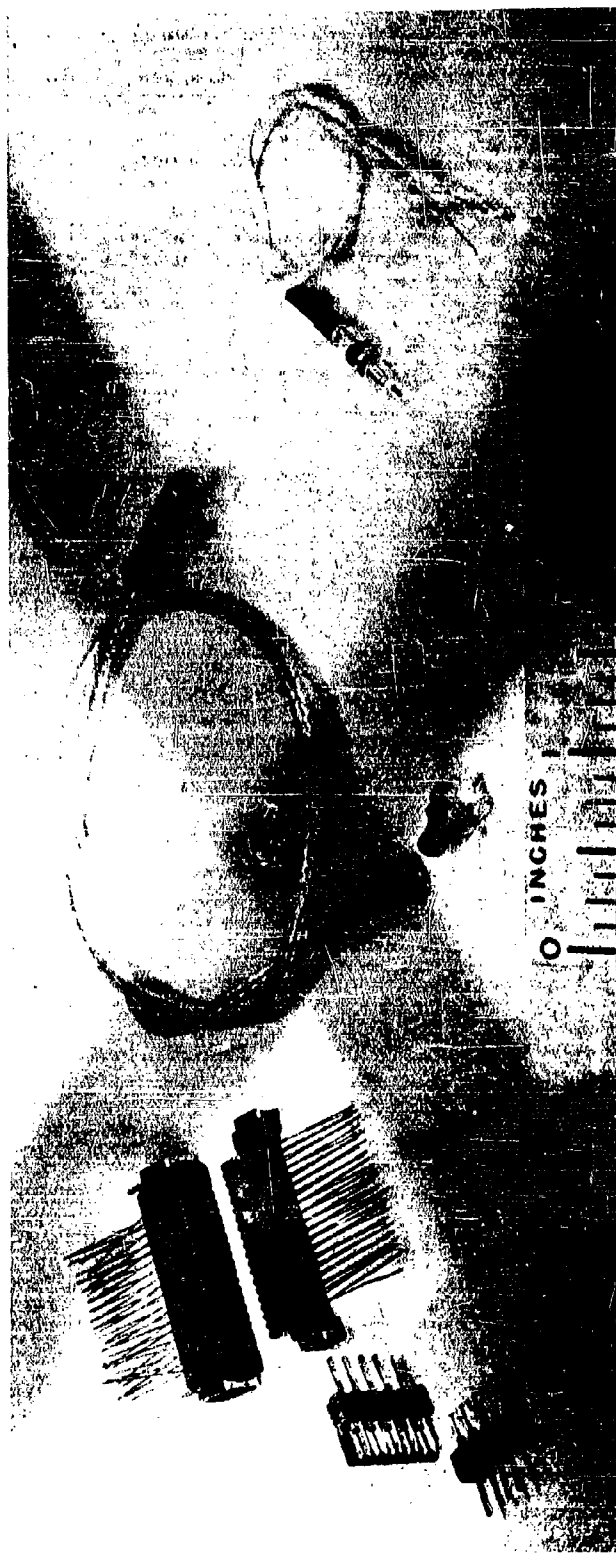


Figure 8. Some commercial connectors available from: lower left, Elco Corp.; upper left, Amphenol Borg Electronics Corp; center, Sealectro Corp; right, Microdot Inc.

Table II. Some commercially available parts suitable for use in microminiature circuits^{1/}

Part	Company	Trade-Name	Dimensions, Inch	Electrical Parameters
CAPACITOR				
Ceramic	Aerovox Corp.	Cerafil	0.320 L x 0.090 D	1000 μ mf
Ceramic	Aerovox Corp.	Cerafil	0.750 L x 0.310 D	0.1 μ f
Ceramic	Aerovox Corp.	Cerol	0.690 L x 0.21 D	0.1 μ f
Ceramic	Aerovox Corp.	Cerol	1.4 L x 0.4 D	2.0 μ f
Ceramic	Erie Resistor Corp.	Weecon Ceramicons	0.15 x 0.15 x 0.10	6 - 3,300 μ mf
Tantalum	P. R. Mallory and Co., Inc.	---	0.310 x 0.310 x 0.035	30 μ f-v
Tantalum	P. R. Mallory and Co., Inc.	---	0.310 x 0.310 x 0.028	15 μ f-v
Ceramic	Mucon Corp.	Narrow-Caps	0.095 x 0.250 x 0.095	100-250-500-700 μ mf
Ceramic	Mucon Corp.	Narrow-Caps	0.095 x 0.300 x 0.095	1000 μ mf
Tantalum	Ohmite Mfg. Co.	Tan-O-Mite T	0.156 L x 0.072 D	ca. 3-12 μ f-v (0.5 to 20 μ f)
Tantalum	Ohmite Mfg. Co.	Tan-O-Mite S	0.187 L x 0.072 D	ca. 4-16 μ f-v (0.5 to 30 μ f)
Tantalum	Ohmite Mfg. Co.	Tan-O-Mite H	0.207 L x 0.066 D	ca. 4-16 μ f-v (0.5 to 30 μ f)
Tantalum	Ohmite Mfg. Co.	Tan-O-Mite M	0.172 L x 0.093 D	ca. 8-32 μ f-v (0.5 to 60 μ f)
RESISTOR				
Composition	Allen-Bradley Co.	TR	0.140 L x 0.067 D	1/10 watt; 10-22,000,000 Ω
Composition	Allen-Bradley Co.	---	0.140 L x 0.020 D	1/20 watt; ---
Ceramic	CTS Corp.	---	0.310 x 0.310 x 0.010	4 watts/in ² ; 10-1,000,000 Ω
Metal film	Daystrom, Inc., Weston Div.	---	0.310 x 0.310 x 0.010	100-250,000 Ω
Pelletized	P. R. Mallory and Co., Inc.	---	0.062 L x 0.1 D	1/10 watt; 5-5,000,000 Ω
Ceramic Film	Microelectron, Inc.	---	0.310 x 0.310 x 0.010	1/2 watt; 10-180,000 Ω
Ceramic Film	Microelectron, Inc.	---	0.062 x 0.025 x 0.100	1/10 watt; 5-1,000,000 Ω
Carbon Metallic	Wilrite Products, Inc.	HM Series	0.156 L x 0.020 D	1/16 watt; 1-100,000 Ω ; 1%
TRANSISTOR				
	Pacific Semiconductors, Inc.	Micro Transistor	0.080 x 0.140 x 0.050 (case)	Equivalent to those of 2N1409, 2N1410, 2N696, 2N697
	Pacific Semiconductors, Inc.	Pico Transistor	0.050 x 0.060 x 0.050 (no case)	
	Rheem Semiconductor Corp.	Microblocc	0.063 L x 0.211 D	2N697
	Sylvania Electric Products, Inc.	Pancake	0.060 L x 0.270 D	2N1684, 2N1782, 83, 84 2N1960, 61, 2, 3, 4, 5, 2N1685, 2N1779, 80, 81, 2N1699
	Texas Instruments, Inc.	umosa	0.050 L x 0.180 D	2N706A, 2N753
	Transitron Electronic Corp.	Microtransistor	0.060 L x 0.160 D	2N839, 40, 41, 42, 43
DIODE				
Probably computer	Microsemiconductor Corp.	---	0.075 L x 0.030 D	Similar to conventional size
Computer	Pacific Semiconductors, Inc.	Microdiode	0.080 L x 0.035 D	Similar to 1N897 thru 902
Computer	Texas Instruments, Inc.	Micro-G	0.060 L x 0.040 D	Similar to conventional size
Zener	Transitron Electronic Corp.	Microregulators	0.080 L x 0.050 D	Zener voltages 5.1 to 12.0 v
Computer	Transitron Electronic Corp.	---	0.080 L x 0.050 D	Similar to conventional size
Temperature Compensation	Transitron Electronic Corp.	Microminiature stabilizers	0.080 L x 0.060 D	Similar to conventional size
LAMP				
Incandescent	Kay Electric Co.	Pinlite	0.062 L x 0.062 D	15 ma at 1.5 v dc
Incandescent	Sylvania Electric Products, Inc.	Mite-T-Light	0.125 L x 0.045 D	35 ma at 1.5 v dc
CRYSTAL				
	McCoy Electronics Co.	Micro Module Crystals	0.28 x 0.28 x 0.075	0.7-200mc

^{1/} The dimensions 0.310 x 0.310 indicate a Micro-module substrate.

Table III. Printing or vapor deposition of multi-component assemblies on a flat insulating substrate, approximate packing density 10^6 to 10^7 parts/in.²

Identification	Approach	Representative Companies	Features	Problems	Circuits Available	Complexity of Construction	Ease of Interconnection
2D ^{1/} original type	Resistor, capacitors, and wiring printed on a ceramic or glass wafer; transistors, diodes, and capacitors inserted in wafer	Aerovox Corp. American Bosch Arma Corp. Globe Union, Inc. Hamilton Standard, Div. United Aircraft Corp. Melpar, Inc. Sprague Electric Co.	1. Available now 2. Maintenance and re- placement of wafers possible	1. Many inter- connections 2. Unproven reliability of parts	Wide tolerance digital and linear	Moderate	Moderate
2D, thin metal film types ^{2/}	Vacuum deposited or sputtered passive components on a ceramic or glass wafer; active components inserted	Bell Telephone Labs. CBS Electronics Haloid Xerox, Inc. Internat'l Resistance Co. Lear, Inc. Motorola, Inc. Philco Corp. Servomechanisms, Inc. Sylvania Electric Products, Inc. Varo Mfg. Co. Westinghouse Electric Corp.	1. Higher packing density than for original 2D 2. Fewer interconnections than for original 2D	1. Limited to smooth flat surfaces 2. Connections to thin films difficult 3. Techniques require small physical tolerance	Wide tolerance digital and linear	Moderate	Difficult
2D, multiple layer thin metal types	Passive components deposited in many layers on a substrate; active components inserted	Int'l Business Machines Varo Mfg. Co.	1. Still fewer interconnections	1. Layerized films increase interconnection and yield problems	Wide tolerance digital	High	Difficult

^{1/} Trade designations: Microvold, Hamilton Standard, Div. United Aircraft Corp.

^{2/} Trade designations: Mu-Circuits, International Resistance Co.

3.1 Original 2D

The original 2D circuit, as developed and designated by DOFL in the year 1957, was so widely described in subsequent years (ref 10 and 16) that it will suffice to say here that it comprised printed resistors and wiring, reduced titanate wafer capacitors, photolithographic transistors and diodes, and a steatite base plate. The principal features that distinguished this circuit from prototype macrocircuits originated by Globe Union, Inc., Centralab Division, were the elimination of the transistor header and the vacuum deposited aluminum leads to the active element. Packing densities greater than 10^6 per cubic inch were obtained in the first 2D modules that were built.

In a recent application of the 2D technique to linear circuits, a 5-stage IF amplifier (ref 17) operating at 30 Mc with 100-db gain and 2-Mc bandwidth has been assembled at DOFL (see Fig. 9). It is packaged in a copper box which has proved adequate for high frequency shielding. Its present packing density is 10^6 parts/cu. ft. For this device, the top of the transistor case was sliced off, leaving the header wires in place, potting resin was poured into the can and a section containing the transistor element was sliced off. The encapsulated element was then inserted in a cavity in the substrate, and leads were fastened to the flush header wires with a silver-filled epoxy resin.

Two hundred 2D binary counters, and a like number of NOR circuits, have been built for DOFL by Sprague Electric Co. These devices employed commercial transistor dice and leads adhered directly to the indium dot by means of painted-on silver-filled epoxy resin. Failure analysis at DOFL has shown that the 12% failures after 600 hours, and additional 4% failures after 4500 hours, were traceable to poor adhesion between the conductive adhesive and the indium dot.

Now that hermetically sealed transistors and surface passivated diodes are commercially available in flat packages (see Fig. 10) new 2D circuits at DOFL are employing these parts. A digital circuit (ref 18) employing these parts, a 1 Mc binary counter having a packing density of 10^6 parts/cu. ft., is shown in Figure 11.

In 2D work at DOFL, one of the problems has always been the time consumed in sandblasting of substrates for the stages of a given prototype device. Therefore, it may be of interest to note in Figure 12 several tools (ref 19) which are now employed at DOFL to turn out ultrasonically impact-ground substrates at a rate much faster than that possible by sandblasting. Pattern definition is also much superior to that obtained by sandblasting.

Commercial availability of active devices such as those shown in Figure 10 opened up the 2D approach for immediate application by

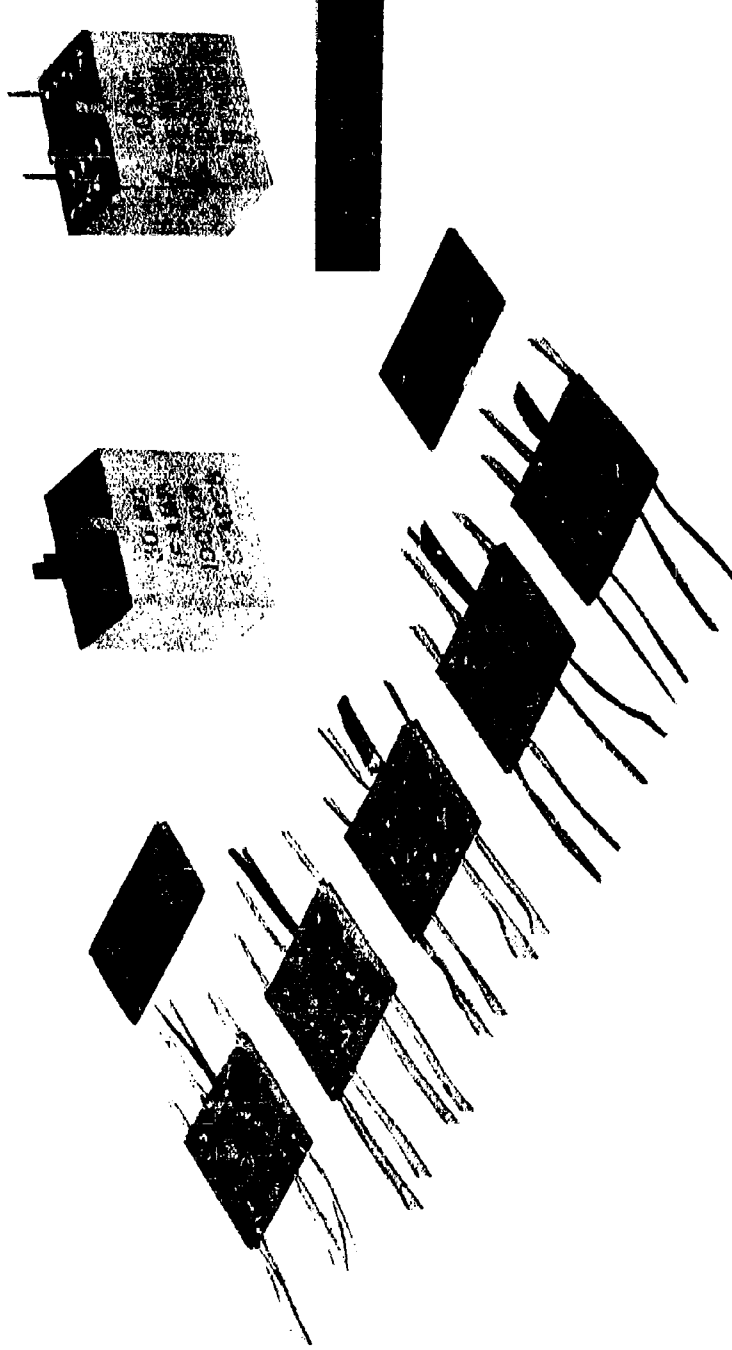


Figure 9. Wafer stages (foreground) for 2D IF amplifier (DOFL) packaged in copper box (top right).



Figure 10. Transistors (Pacific Semiconductors, Inc.) suitable for use in 2D assemblies: left, surface passivated and dipped; right, similar unit encased.

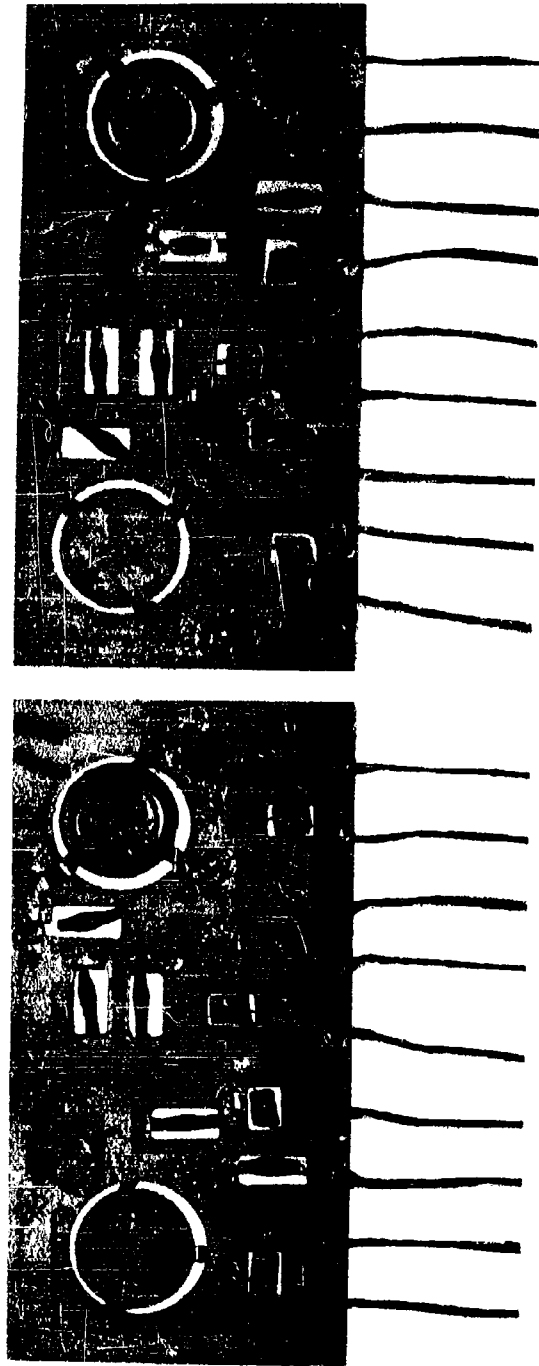


Figure 11. 1-mc binary counter (DOFL) constructed by 2D techniques but employs commercial hermetically sealed or surface-passivated active parts.

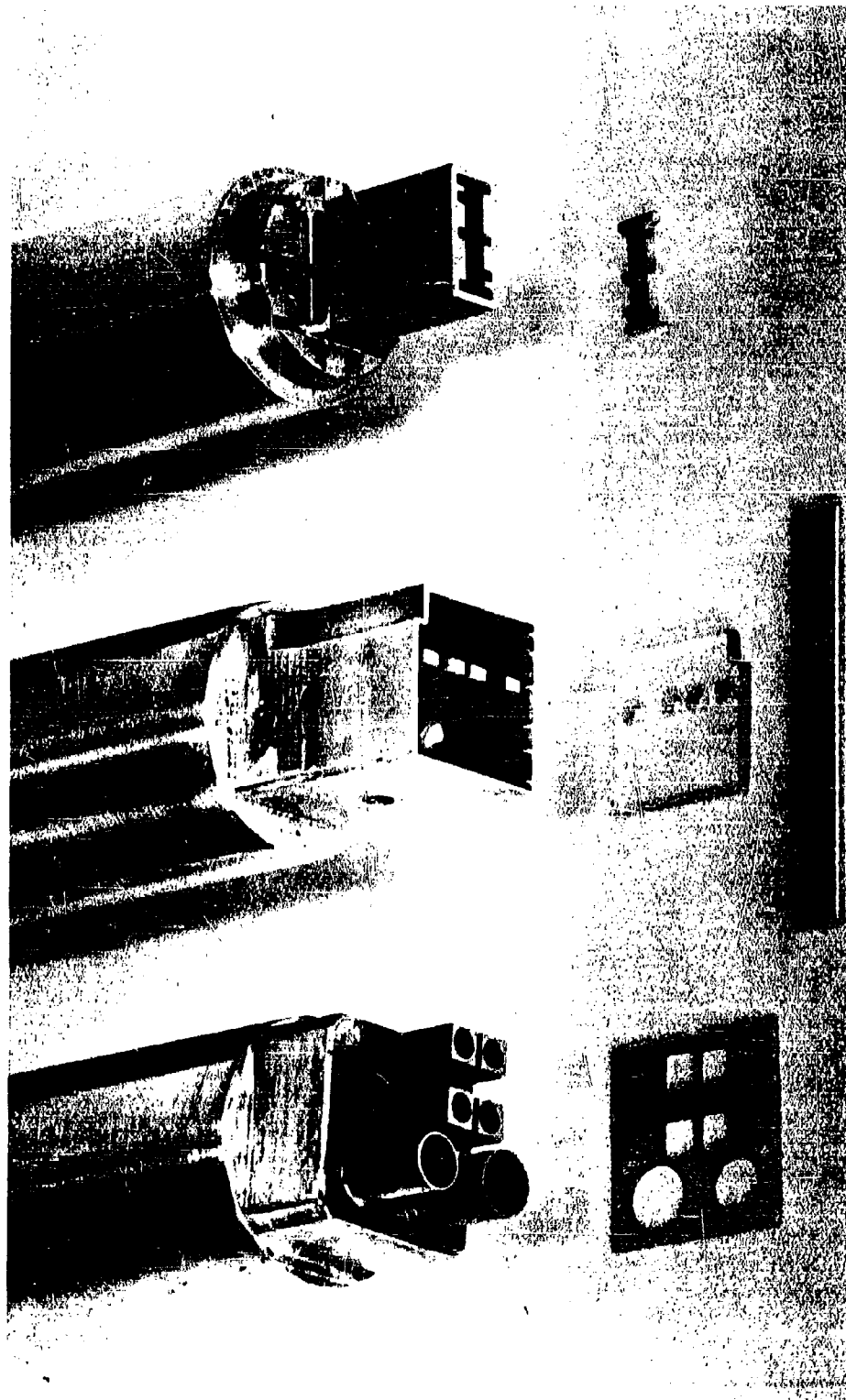


Figure 12. DOFL-designed tools (background) for ultrasonic impact machining of (foreground, left to right) 2D ceramic substrate, 2D glass substrate, and a Hall-effect specimen.

all companies equipped to print passive components in thin-film form. Variations in the usual techniques appear in the PEC's (packaged electronic circuits) and Micro-circuits of Centralab Division of Globe Union, Inc. and Sprague Electric Co., respectively, each of which use a ceramic substrate to serve both as the base and the capacitor dielectric, and apply screened resistors and inserted active parts.

Instead of using soldering or welding techniques of interconnection in 2D circuits, Hamilton Standard is using electron beam welding techniques because they permit welding even closer to components than do conventional welding methods. Figure 13 shows such a welded circuit. The alumina substrate is 0.75 x 0.50 x 0.025 inch in dimensions and bears printed resistors and wafer capacitors which are welded to connector pins placed along one edge. A later model uses all-deposited passive components. Plans for mechanized production of a 25-stage computer module are in progress.

3.2 2D thin-metal-film types

The above-described modifications of the original 2D technique, although immediately producible and salable, have little potential for packing densities higher than about 10^6 parts/cu. ft. Therefore, many of the companies that are supplying equipment made by these techniques are also actively engaged in development of true extensions of the original 2D technique, namely incorporation of thin-metal-film parts other than the conductors. As indicated in Table III, packing densities of 10^7 can be expected and, in addition, metal-film parts should be much more stable than their organic-film counterparts.

The logical sequence of events in the extension of the 2D technique involves first the formation of thin-metal-film passive parts by such techniques as vacuum or chemical deposition, sputtering, photolithography, etching, and combinations of these methods, and then the formation of thin-metal-film active parts. Such circuits are conceived to be only a few years away while cheap, reliable, integrated and functional circuits, to be considered in the next section, are probably seven to ten years away (ref 20).

To date, conductors and resistors are the principal parts being laid down in commercially available thin-metal-film circuits. The International Resistance Co. vacuum deposits resistors on both sides of a glass or ceramic wafer, and inserts the active components in an aperture in the wafer. Figure 14 shows an IRC three-stage audio amplifier, comprising three cased commercial transistors, one diode, and three resistors on a glass plate. The leads of two of the transistors are soldered to one side of the plate and those of the third transistor to the reverse side. IRC is also using uncased transistors in some of their thin-metal-film circuits. They are now exploring the



Figure 13. 2D-type circuit (Hamilton Standard Div., United Aircraft Corp.) assembled on alumina wafer by electron beam welding techniques.

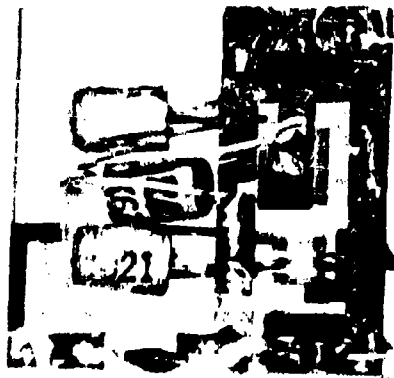
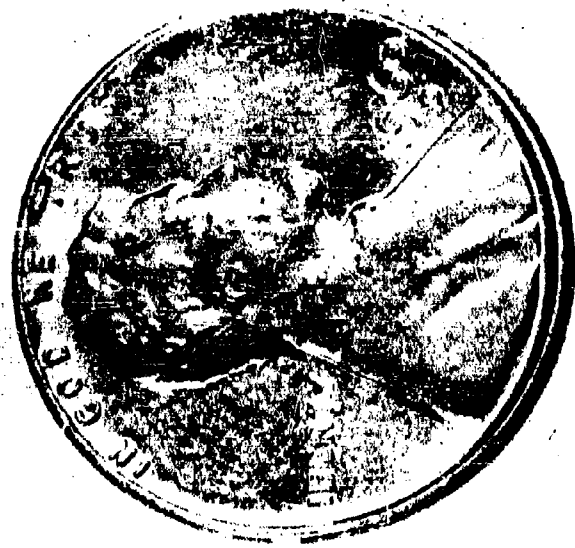


Figure 14. 2D thin-metal-film circuit (International Resistance Co.) with attached active parts; a three-stage audio amplifier.

possibilities of thin films made from mixtures of two or more materials evaporated simultaneously or alternately, and of thin-film inductors which it is hoped can be produced with inductances ranging from 40 microhenries to one millihenry (ref 21).

Figure 15 is included to show the unusual type of resistor pattern developed by Lear, Inc. in its approach to thin-metal-film circuitry. For its high-valued resistors, Lear uses a paralleled pattern, rather than a meander pattern, because the former pattern lends greater strength and rigidity to a thin-metal mask than does the meander pattern.

The number of electronic companies engaged in research work in thin-metal films is burgeoning. Servomechanisms, for example, has made experimental circuits comprising vacuum deposited nickel-iron conductors, nichrome resistors, and uncased active elements. An interior view of their vacuum chamber and 16-position mask used in pilot-lot production of flip-flops is shown in Figure 16. CBS Electronics uses vacuum or chemically deposited conductors made of aluminum, chrome-gold, or copper-gold, and silicon monoxide thin-film capacitors with aluminum or gold electrodes. Examples of experimental vacuum deposited circuits made by General Electric Co., and by DOFL (ref 22), are shown in Figures 17 and 18, respectively. Both employ chromium gold-overlaid conductors, nichrome resistors, silicon monoxide capacitors and attached active parts. The DOFL circuit is, again, the 2D IF amplifier which was shown in Figure 9 in the original 2D-type of construction.

Haloid Xerox (ref 23) has an interesting scheme which avoids any necessity for designers to send proprietary circuit diagrams to the manufacturer for construction. They provide RC-circuit ceramic plates on which films of aluminum or nickel for conductors, chromium for resistors, and silicon monoxide for capacitors have been vacuum deposited in successive layers without any attempt to outline conductor or resistor areas. Equipment producers can selectively etch these plates to the desired pattern. If the plates are notched, and the notches metallized, they can then be inserted in printed circuit boards, thereby eliminating soldered wire connections.

Sylvania Electric Products, Inc. (ref 24) is also promoting a combination of the thin-metal-film techniques with the Micro-module approach to yield a package which they call a "Microminiature Module." In it, each of the several 0.5-inch-square alumina wafers accommodates a variety of thin-film passive parts, and a complete function. Wafers have protruding conductive tabs on all sides. After hermetically sealing wafers between spacer frames, these tabs are inserted in Fotoceram printed circuit boards on all four sides of the stack. Current construction gives a parts density figure of only 6×10^5 /cu. ft. Since the package lends itself to eventual incorporation of integrated and functional circuits, this parts density figure is

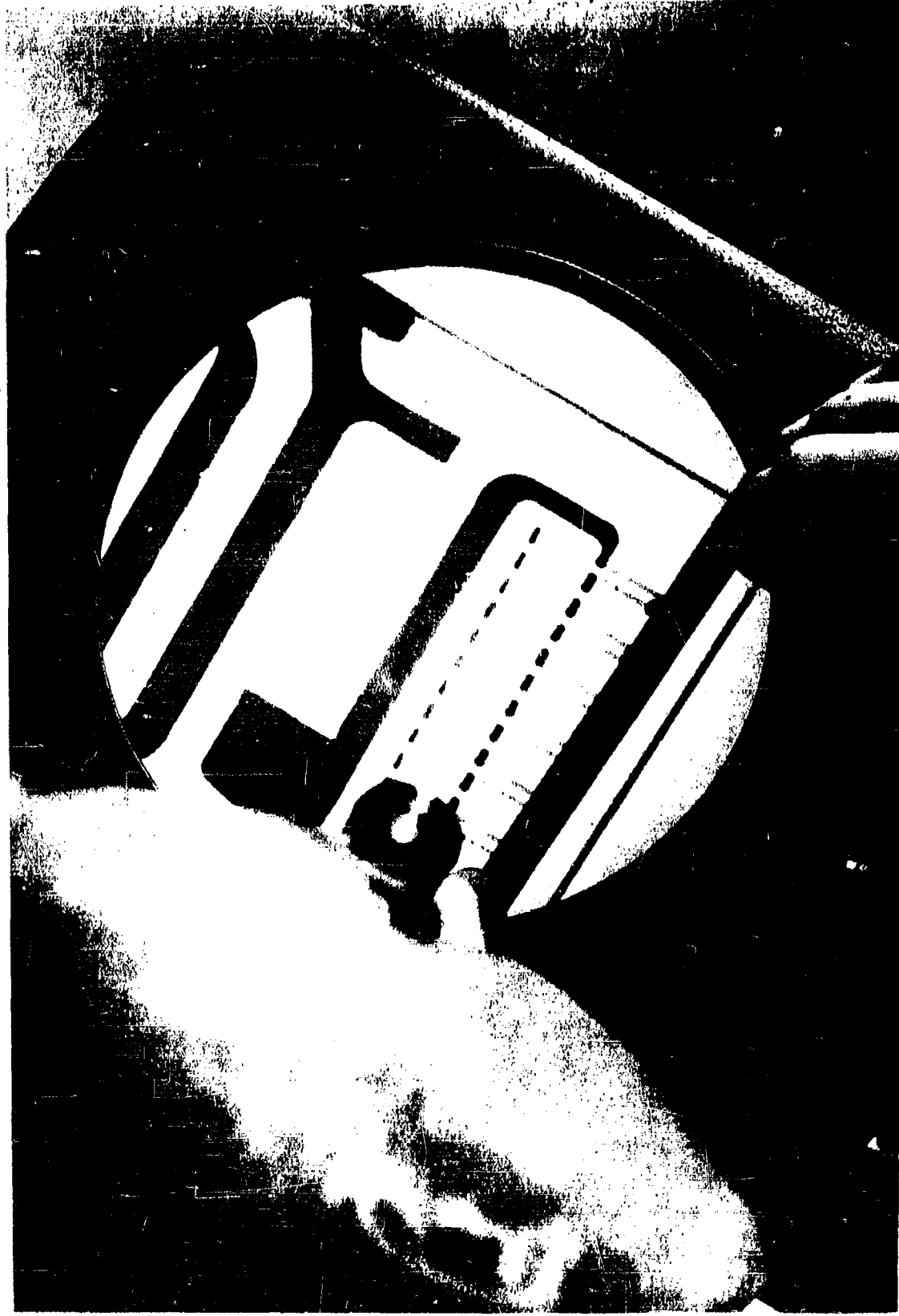


Figure 15. 2D thin-metal-film resistor pattern (Lear, Inc.).

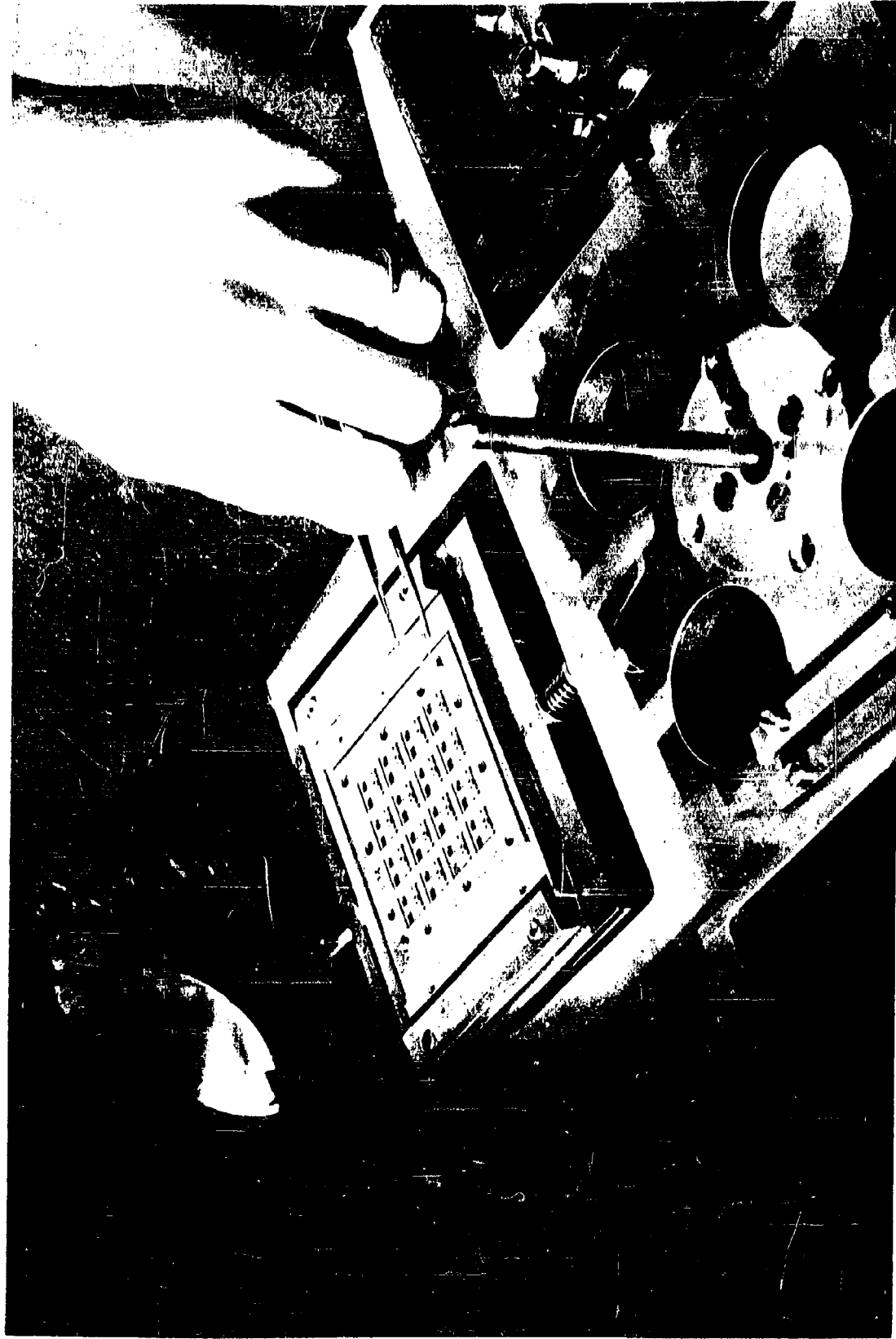


Figure 16. 16-position conductor mask (Servomechanisms, Inc.) for use in pilot-lot production of 2D thin-metal-film flip-flops.

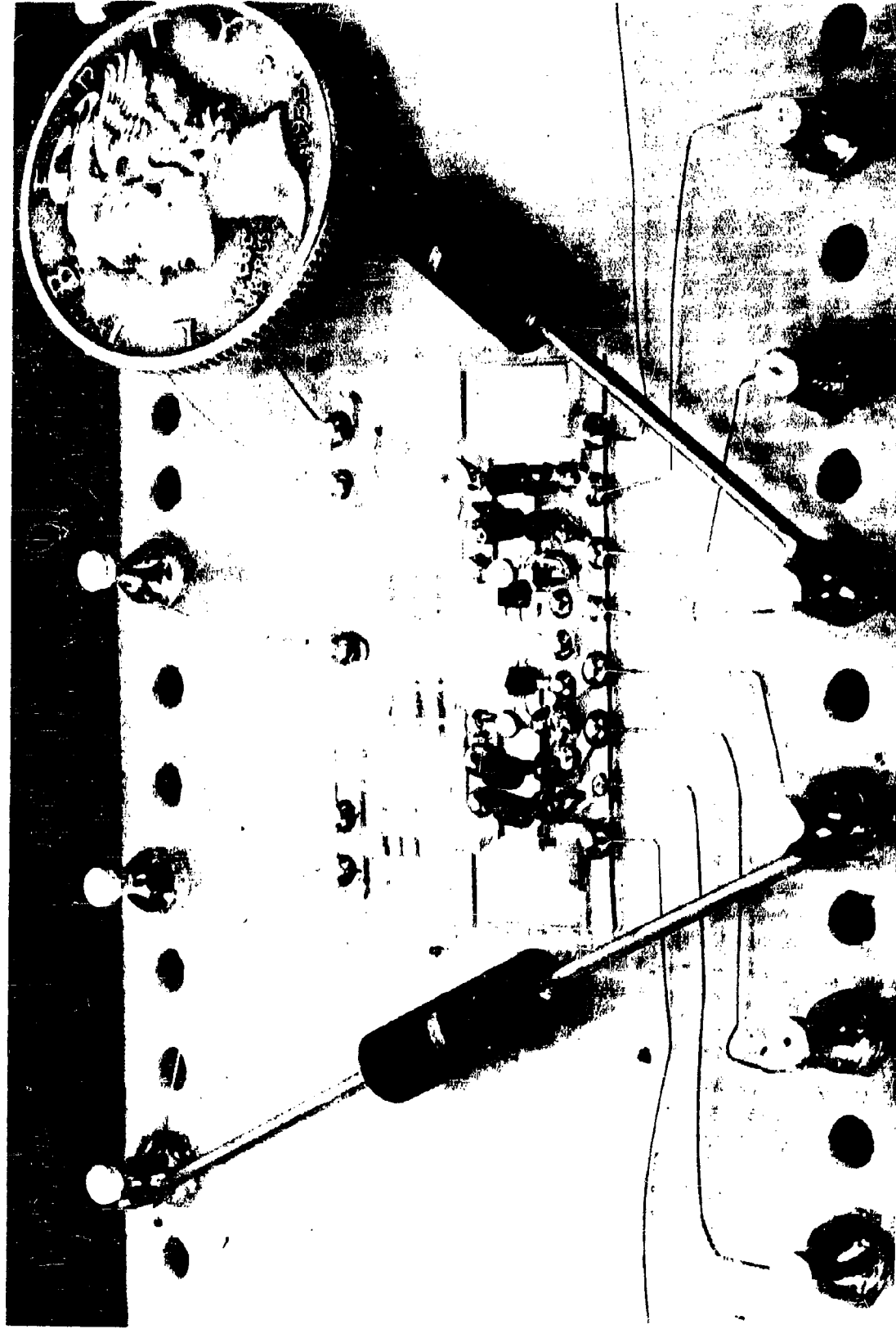
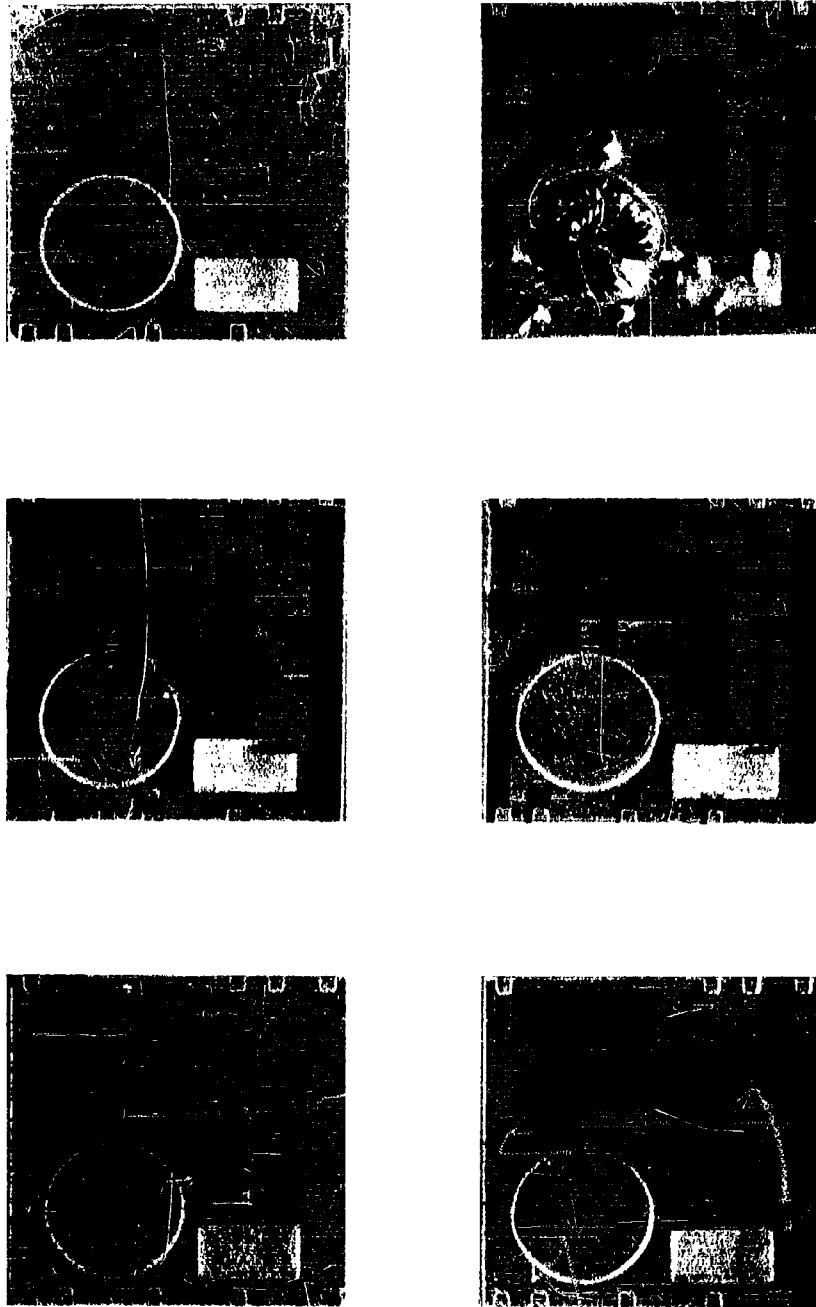


Figure 17. 2D thin-metal-film circuit (General Electric Co.) employing vacuum deposited conductors, resistors, and capacitors, and attached active parts; double NOR mounted on a terminal board with external load resistors.



672-61

Figure 18. 2D thin-metal-film circuit (DOFL) employing vacuum deposited conductors, resistors, and capacitors, and attached active parts: from top left to right, substrate with resistors, with conductive wiring, with dielectric film (invisible), with counter electrode, composite of previous films, and composite with inserted coil and transistor; IF amplifier.

not fixed. Sylvania suggests that eventually the criterion of degree of miniaturization will be in terms of stages or circuit functions per cu. ft., rather than in terms of parts per cu. ft.

In 1959, Bell Telephone Laboratories (ref 25) reported the sputtering of refractory metals, in particular tantalum, to form resistors, capacitors, and conductors on a glass or ceramic substrate. The resistors, capacitor anodes, and most of the interconnections were laid down in a simultaneous operation. The principal advantage of the method is probably the unquestionable reliability of the connections. Disadvantages compared with vacuum deposition techniques include the much longer length of time for deposition, and the exaggerated problems in purity of films. Multi-layer sputtered films were envisioned in 1959 but as far as is known have not been the subject of much investigation.

The general area of chemically deposited passive parts is thus far almost untouched. In comparison with vacuum deposition, chemical deposition has the advantage of reduced cost, in part because parts can readily be deposited simultaneously on both surfaces of the wafer. Lockheed is working in this area, and so is DOFL. Figure 19 shows an amplifier with a current gain of 100 constructed at DOFL (ref 26) by chemical and electrochemical techniques. This amplifier comprises five chemically deposited nickel-phosphorous resistors, conductors of electroplated copper over chemically deposited nickel, two commercial surface-passivated transistors, and a DOFL micro-lamp (ref 27) which is produced commercially by Kay Laboratories and by Sylvania.

3.3 2D multiple-layer thin-metal-film types

At least two companies, IBM and Varo Manufacturing Co., are actively investigating multi-layer vacuum deposited thin-film circuits. IBM (ref 28) reported a feasibility study in which six different circuits were constructed from caseless commercial active components, miniature bulk-type wound inductors, and vacuum-deposited layered passive components. Resistors were made from nichrome, conductors from aluminum and capacitors in most cases from silicon monoxide. The number of layers varied with the particular circuit. As an example, an OR circuit employed one layer each of undercoat and overcoat (silicon monoxide), four layers of resistor film (NiCr), four layers of resistor lands (aluminum), four layers of insulating film (silicon monoxide), one layer of dielectric film (silicon monoxide), one layer of connector pattern (aluminum/chromium), and one layer each of bottom and top plate (aluminum). Connections between the thin films and active elements or other circuitry were made by thermal compression bonding. Parts density figures of 3×10^6 per cu. ft. were achieved in the first models and operating circuits were produced. However, some of the circuits, when packaged in stacked form, overheated when operated at an ambient temperature of 140°F. The thinness of the insulators also presented some problems.

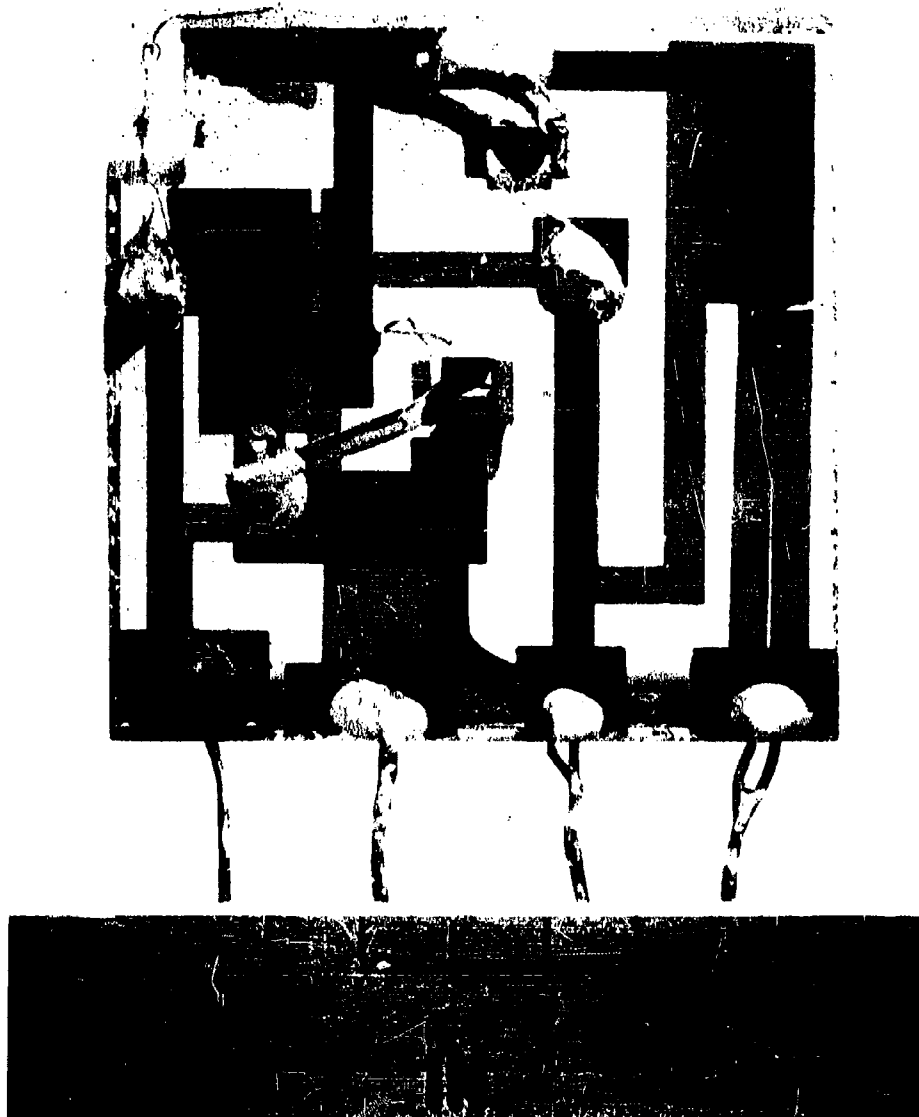


Figure 19. 2D thin-metal-film current amplifier circuit (DOFL) employing five chemically deposited nickel-phosphorous resistors, two commercial transistors, and a DOFL microlamp (upper left-hand corner of wafer).

648-61

Varo Manufacturing Co. has also investigated multiple-layer film techniques and feels that the limiting factor is not the number of layers but rather the heat dissipation factor (ref 9). Varo specifies a limit of 1 w on a 1-inch-square uncooled substrate.

In the past year, an increasing amount of research work on 2D-type active parts is also being reported. IBM investigated the possibility of growing thin single-crystal layers of silicon, with controlled electrical and physical properties, by an epitaxial vapor growth process. In this process, single-crystal silicon was deposited from silicon iodide vapors onto single-crystal silicon at a temperature of about 900°C and impurities (boron, phosphorous, arsenic, or antimony) from a silicon-impurity alloy source were simultaneously incorporated in the lattice. Multiple junctions of P, N, P⁺, and N⁺ conductivity types were grown and feasibility established but the need for refinements was also clear. IBM has also investigated germanium and intermetallics in the preparation of multilayer semiconductor sandwiches. So far it seems to be conceded that the transistors are not very good (ref 29). Bell Telephone Labs. is also working in this area and in 1960 announced an nipn film transistor which is thought to be made by reduction of silicon tetrachloride in hydrogen.

Another recent area of investigation is that of thin-film active parts which are based on quantum mechanical tunneling of electrons from a metal through a thin (< 100 Å) insulating film to a collector of electrons. If the band structure of the collector is of a suitable nature, then the Esaki negative-resistance characteristic is obtained. Such parts presumably operate at room temperature, exhibit high-speed switching, and are more radiation resistant than are conventional transistors and diodes. Stanford Research Institute proposed designs for tunnel-effect vacuum triodes and tetrodes, and for memory devices employing such parts. At least a half dozen companies have designed switching or other applications employing gallium-arsenide tunnel diodes. Republic Aviation Corp. has described (ref 30) a thin film tunnel diode made from titanium, the top surface of which is anodized and this film in turn covered with a counter electrode. Since Republic is also working on titanium thin-film capacitors and resistors, it hopes to produce a complete microminiature circuit in one manufacturing operation by several deposition and oxidation steps.

Philco Corp. has just announced (ref 31) a thin-film three-terminal tunneling device. Its structure is reported to be aluminum/aluminum oxide/aluminum/germanium. Experimental units have shown collector efficiencies between 75 and 90% and transconductances of over 2500 μmhos.

3.4 Other 2-D-related work

Impetus for supplementing or replacing conventional vacuum deposition techniques with electron beam techniques is increasing.

Such advantages as preparation of the substrate so as to enhance the chance of semiconductor crystal film deposition, vaporization and deposition of refractory materials which are presently impossible to evaporate with conventional hot-crucible techniques, machining of vacuum deposited films to a precise pattern, and joining or alloying at precise points are visualized (ref 32). For the several applications, beams variable from coarse (0.030 - 0.100 inch diameter) to fine (.001 to .0001 inch diameter), ultra-high vacuums (down to 1×10^{-10} mm), and means of positioning the beam at any precise point within a working circle of about 0.75 inch diameter may be needed. Carl Zeiss Corp. and the Alloyd Corp. have developed first-generation-type electron beam equipment for use in the microminiaturization field. Generally speaking, this whole area is wide open for investigation.

Another area of current investigation stems from the aforementioned heat dissipation problems in densely packed circuits. Snyder (ref 33) has recently examined the chemistry of thermoelectric materials, i. e., materials which become heat sinks when an electric current is passed through them in one direction and become heat sources when it is passed in the reverse direction. He notes that good thermoelectric semiconductors are composed of elements differing greatly in atomic weight and that they have high molecular weight and low lattice elastic constants (i. e., a low Debye temperature). In addition, the ratio of carrier mobility to lattice thermal conductivity apparently increases with increasing average atomic weight of the elements and may be increased by incorporating impurity atoms of differing atomic weight but similar chemical properties. Bi_2Te_3 is one of the earliest and best known of the thermoelectric semiconductors.

Although the majority of commercial applications of these materials has thus far been in electrical generators, research in cooling applications is also well under way. For cooling electronic parts, General Thermoelectric Corp. is offering a quaternary semiconductor alloy made of bismuth, tellurium, selenium, and antimony, and also a module of eight thermocouples called a "Frigistor." This device is about $1 \times 1 \times 0.25$ inch and has a heat pumping capacity of 10 to 15 watts. It permits h f germanium transistors to operate at 150°C and silicon power transistors up to 300°C . Materials Electronics Products Corp. offers thermoelectric semiconductor elements ranging in diameter from 3 to 38 mm. The largest commercial effort is probably that of Westinghouse which has demonstrated units for cooling various sizes and types of transistors. They have in progress an investigation of rare earth thermoelectrics and have reported (ref 34) that cerium and samarium sulfides have excellent high temperature stability and good thermoelectric efficiencies at temperatures as high as 2000°F .

DOFL's contribution (ref 35) in this area is shown in Figure 20. Its unique feature is the use of etched circuits to simplify fabrication. The aluminum-alloy anodized base plate and cooling chamber bear solder-covered etched circuits. These pieces are assembled in a

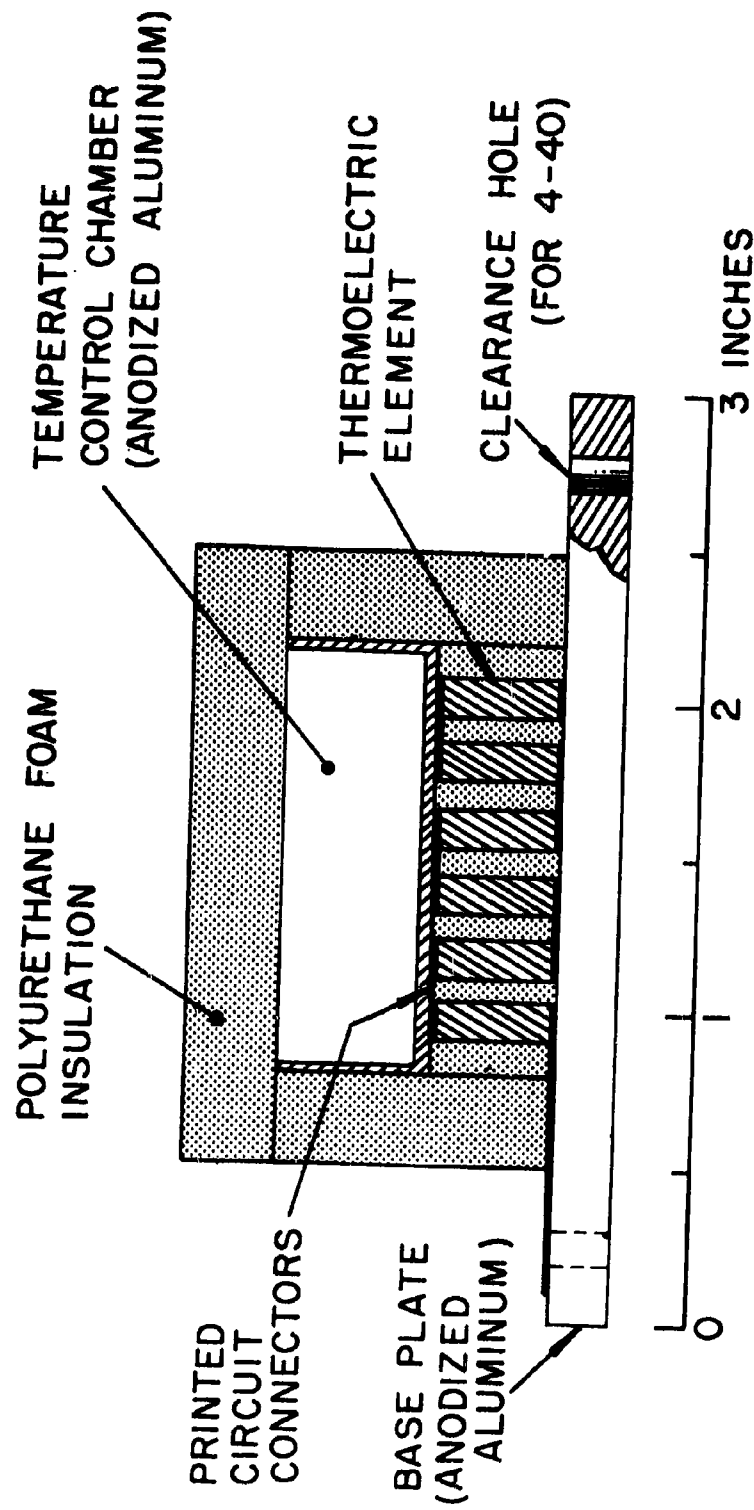


Figure 20. Thermoelectric temperature control device (DOFL) uses commercial semi-conducting elements and etched circuit connectors.

jig with tinned thermoelectric commercial elements in place in the baseplate. When the solder is melted, connection is completed. Use of 1/8-inch-diameter elements permits operation at 2 volts and 3 amperes to give a temperature reduction of 45°C.

4. PREPARATION OF COMPLETE CIRCUITS FROM A SOLID BLOCK OF SEMICONDUCTOR MATERIAL

In Table IV, this section is divided into integrated and functional circuits. For purposes of this discussion, integrated circuits are defined as circuits in which component parts are formed in a block of semiconducting material with a 1:1 correspondence between the semiconductor part and a conventional component part that performs the same function. Integrated circuits will also include circuits in which component parts appear on more than one block of semiconductor material, because it will be shown that in some cases these circuits operate better when subdivided. Functional circuits are defined as circuits which attempt to use the functions associated with multi-layer semiconductor devices to achieve the same input-output relationships that the integrated designer achieves with a multiplicity of integrated parts.

4.1 Integrated circuits

First-generation-type integrated circuits were first announced about two years ago. They comprise a complete circuit fabricated in or on a block of semiconductor material by means of 15 to 20 steps that include such techniques as oxide masking, diffusion, metal deposition, alloying, and surface shaping. Resistors can be obtained from properly doped bulk material or from thin surface layers formed by diffusion techniques. Capacitors can be obtained from a reverse-biased pn junction, where the depletion region at the junction serves as the dielectric, or from a sandwich built up by depositing a layer of silicon oxide on the top surface of the semiconductor material and a layer of metal on top of the silicon oxide. Active parts can be fabricated either by diffusion or by alloying.

The procedures employed by Texas Instruments Co. (ref 36) in making an integrated NOR circuit are shown schematically in Figures 21 and 22. Although this circuit can be designed on a single silicon wafer, in practice it has been found desirable to separate the resistors in the input circuit from the load resistor. Hence, all the resistors are actually formed from two pieces of material. The final step is to provide input and output connections, and jumpers of thermally bonded gold wire between internal elements.

The network shown in Figure 22 has a packing density of the order of 10^8 parts/cu. ft. When thirteen of these networks were interconnected in an operating assembly, the packing density dropped to 10^7 parts/cu. ft. At these figures, heat dissipation is critical and it

Table IV. Complete circuits, integrated and functional, approximate packing density 10^6 to $> 10^8$ equivalent parts/in.³

Identification	Approach	Representative Companies	Features	Problems	Circuits Available	Complexity of Construction	Ease of Interconnection
Integrated	Active and passive parts are designed in a semi-conducting material by such techniques as oxide masking, etching, diffusion, metal deposition and surface shaping. The number of individual components in the semiconductor matches that in a similar conventional circuit.	Fairchild Semiconductor Corp. Radio Corp. of America Raytheon Co. Sperry-Rand Corp. Texas Instruments, Inc.	1. Few process steps 2. High inherent reliability 3. Few interconnections	1. Component values are restricted 2. Tolerances difficult to check 3. Costly 4. Temperature dependent devices	Wide tolerance digital	High	Moderate to very difficult depending on lead configuration and packing density
Functional	Multi-zone semiconductor crystals are designed to yield a circuit function which therefore has been achieved with a multiplicity of parts.	Westinghouse Electric Corp.	1. Enormous packing densities 2. Low power requirements 3. High inherent reliability	1. Long range research required 2. Costly 3. Temperature dependent devices	Wide tolerance digital and linear	High	Moderate to very difficult depending on lead configuration and packing density

Trade designations: Semi-Nex, Sperry Rand Corp. Solid Circuits, Texas Instruments, Inc.

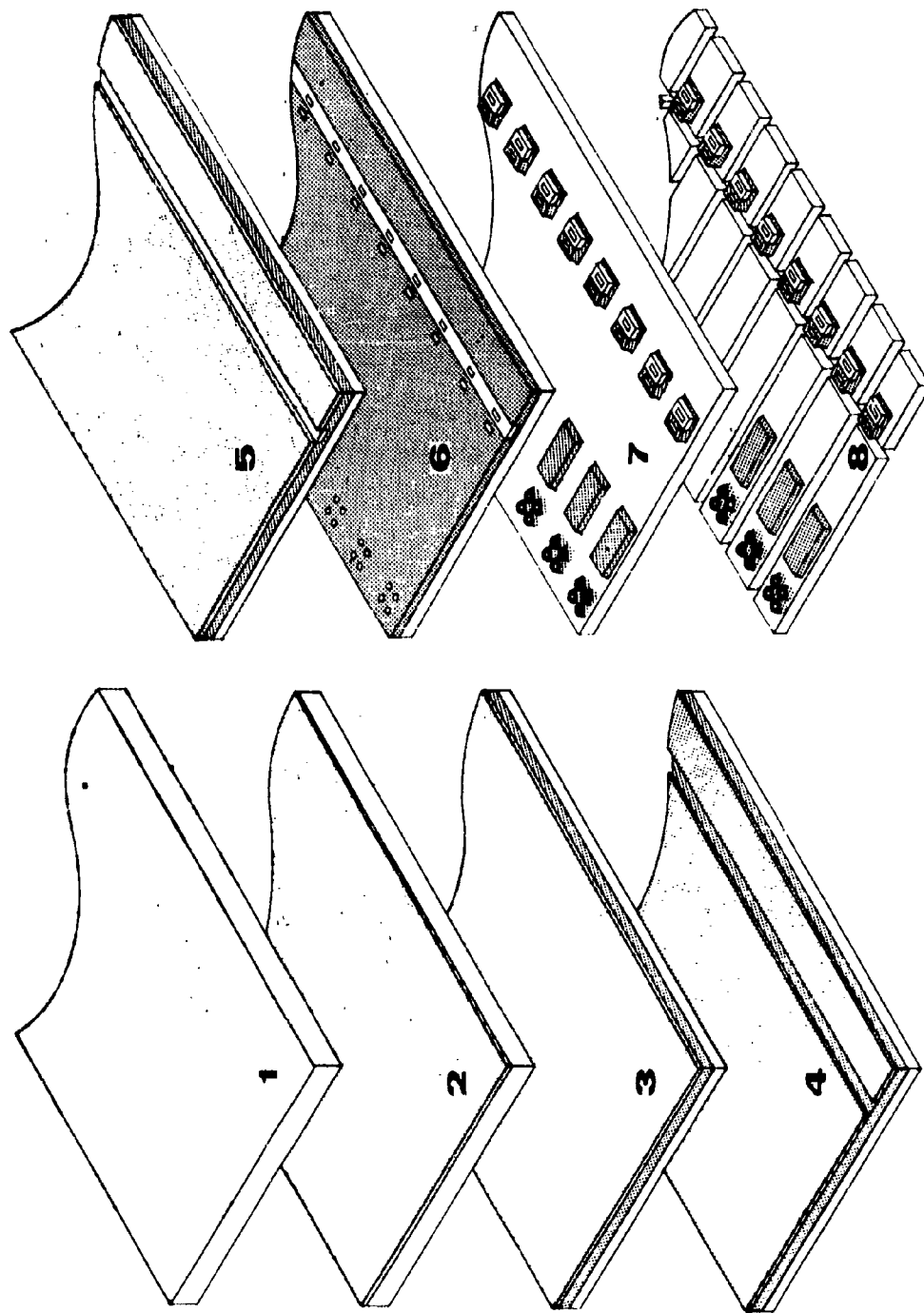


Figure 21. Steps in fabrication of NOR logic element (Texas Instruments, Inc.): (1) Clean n-type silicon wafer, (2) surface oxidized, (3) p-type diffused thru oxide, (4) oxide selectively removed, (5) n-type diffusion for emitter, (6) oxide removed and metal contacts applied, (7) unwanted p-type removed by selective mesa etch, and (8) networks separated.

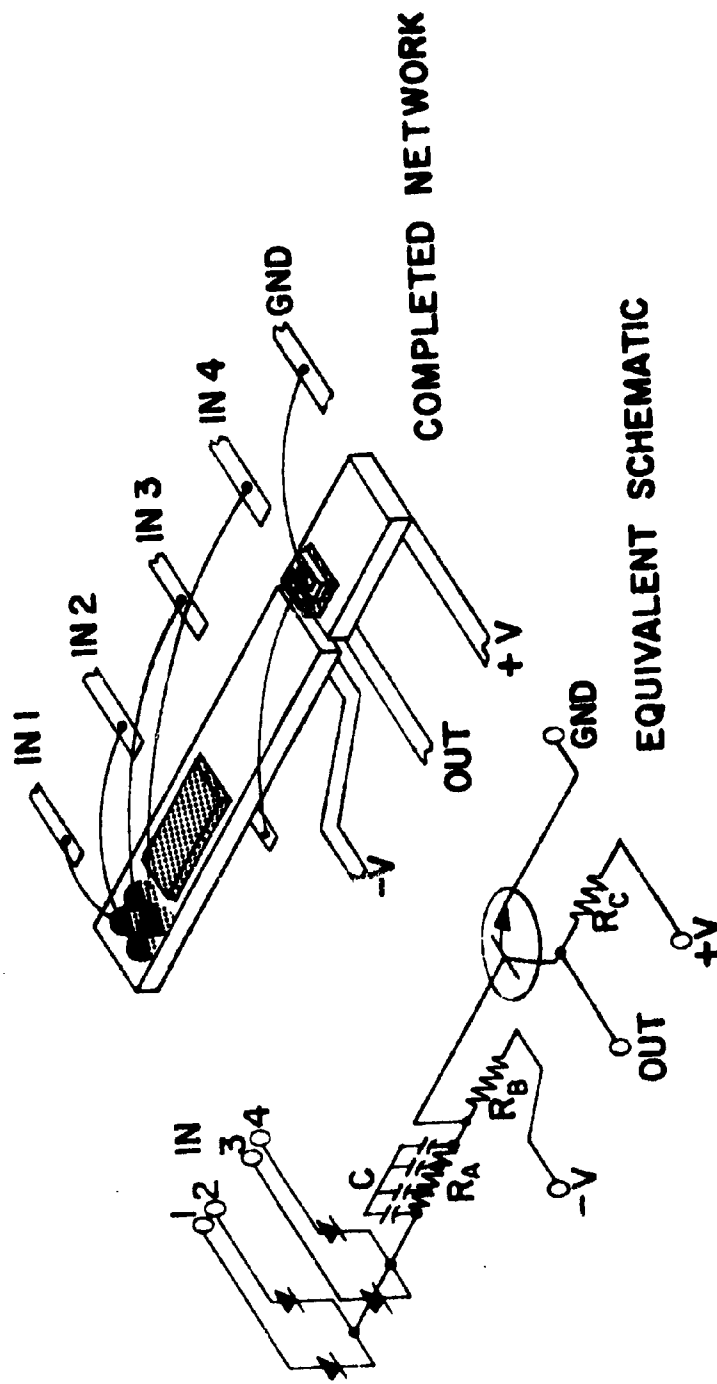


Figure 22. Integrated circuit (Texas Instruments, Inc.): right, network made from NOR logic elements shown in Figure 21; left, equivalent circuit.

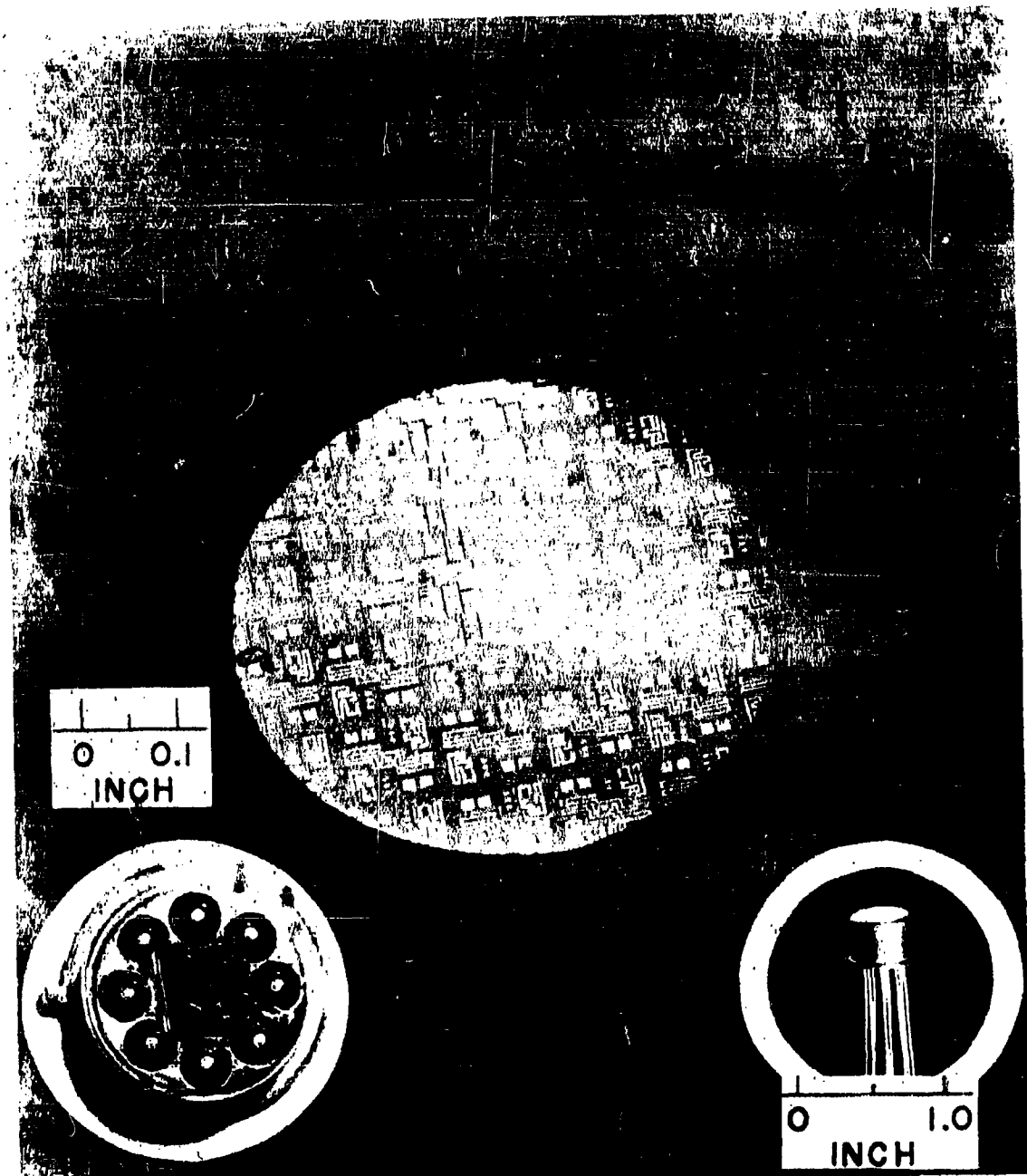
is essential to design the network for minimum power consumption, to shape the package to have a high ratio of surface area to volume, and to incorporate conduction paths to heat sinks, or to cooling devices such as those discussed in the preceding section.

Merck, Sharp and Dohme are producing experimental integrated circuits. Their procedures (ref 37) feature vapor phase reduction of a volatile silicon derivative with hydrogen, and simultaneous doping, to yield relatively thick layers of single-crystal silicon on a single-crystal silicon substrate. Merck points out the advantages of being able to position either highly conductive paths or isolation layers at will deep within the structure. Laminar layers which are controlled in conductivity type, resistivity, and thickness result. For example, Merck has designed a relaxation oscillator from nine layers: (1) base, or support and isolation layer, (2), (3), (4), (5), and (6) alternating P^+ , P , N , P , and N^+ layers to form a pnpn switch, and layers (7), (8) and (9) alternating P^+ , N , and P layers to form capacitive and resistive diodes. Devices were isolated by masking and etching. Merck also points out that their techniques can be combined with the technique of oxide masking, diffusion, and alloying to expand the possibilities in microcircuit elements.

Sperry Rand Corp. is also engaged in research in integrated circuits. At the top of Figure 23 there is shown a pattern produced on a slice of silicon by photoresist masking and diffusion of an impurity through the mask. The intersections of the junctions at the surface of the slice are passivated. Additional masking, diffusion and evaporation produce passive parts and then individual dice are cut out and mounted on a miniature transistor can header as shown on the left hand side of Figure 23. The completed device, shown on the right in this same figure, is made up of two transistors, four diodes, and three resistors. One feature of the Sperry technique is that internal interconnections are made through the block itself so that thermal compression bonding is required only between the header pins and the terminal points on the dice.

Fairchild Semiconductor Corp. is using a combination of the Texas Instruments circuit approach and the Sperry packaging approach and should be credited with the original concept of marketing a compatible family of integrated digital circuits in TO-5 transistor cans. They are now conducting research directed toward elimination of thermal compression bonding in favor of vacuum deposited connections.

Burroughs Corp. is studying structures (ref 38) consisting of: (1) a glass or ceramic circuit plate bearing screened multi-element connectors and (2) an array of single-process mesa diode-bearing silicon strips. A conductive coating is first applied over the silicon wafer, and then it is ultrasonically machined into a group of electrically isolated strips. After machining, the coating carries the connection around the end of the strip. The circuit plate is attached to the wafer, the junctions are etched, washed, and passivated, and the device is



708-61

Figure 23. Integrated circuit (Sperry Rand Corp.) made from a block of silicon: background, sixteen-dice slice; lower left, a die mounted in an 8-pin header; lower right, encapsulated device containing two transistors, four diodes, and ten resistors.

encapsulated. The first product is a binary coded decimal-to-decimal converter consisting of forty diodes and interconnections and packaged in a volume of 1 x 0.6 x 0.313 inch. Since the large numbers of diodes in a single package are processed under identical conditions, variations among the diodes are reduced to a maximum.

Raytheon Co. is investigating integrated silicon circuits produced primarily by alloying and post-alloy-diffusion methods. Presumably these methods sacrifice precise control of geometry for gains in reliability, yield, and economy. However, problems of surface recombination effects and surface passivation are exaggerated (ref 9).

An integrated-type circuit constructed (ref 39) at DOFL is shown in Figure 24. It is a common emitter amplifier, and gains for such circuits have ranged from 15 to 50. The transistor (lower left) with electrodes 0.002 inch x 0.006 inch was made on one piece of germanium. It was then mounted on a Jetec 30 header, together with a semiconductor slice (top) containing four resistors made from the diffused skin of the semiconductor, and one transistor. The resistors and separate transistor were connected by means of thermal compression bonded leads.

Because the germanium slice was originally designed for a NOR circuit, some excess parts appear on the slice; of the five parts, only three resistors are being used, two in series. Leakage paths between the resistors and the transistor in the germanium slice made it necessary to separate the transistor from the resistors. This difficulty is probably similar to that encountered by Texas Instruments before their resistors were separated onto two wafers. Such difficulties must be resolved before either of these circuits can be considered truly integrated.

Wallmark (ref 40) has considered the limitations of integrated devices: (1) the physical size at which it is not possible to handle less than an entire system without as yet unknown tools, (2) the previously mentioned heat dissipation limitation, and (3) the probability that accidents in the fabrication processes will result in loss of an entire unit. He concludes that the decreased volume and weight and smaller number of interconnections of these devices compared to conventional component-part-assembled devices have to counterbalance the higher fabrication losses, and that these losses must be minimized by: (1) designing circuits so as to balance the extent of integration against the losses, (2) investing more heavily in the fabrication process on the basis that the integrated device will be higher priced, and (3) developing means of doctoring faulty devices, for example, by providing reserve stages and using them to bypass faulty stages.

4.2 Functional circuits

In producing functional circuits, the desired electronic function is conceived at the outset and then designed in multiple-junction



Figure 24. Integrated circuit (DOFL) mounted on a 3-pin header: lower left, a germanium transistor; top a germanium slice containing resistors.

semiconductor material. As an example of circuit redesign, if an ac-to-dc converter were required, it could be built from conventional parts (transformer, rectifier and three filter components) as shown on the left-hand side of Figure 25. On the other hand, it could be built from a block of semiconductor material as shown on the right-hand side of this figure. In the latter case, when ac is applied to the resistive domain, heat is passed through the center domain, which is an electrical insulator but a thermal conductor, and then dc is generated by the thermoelectric domain. The output has no ripple because the rate of heat flow to the thermoelectric domain is uniform.

Westinghouse (ref 41) has built thus far eight classes of functional blocks at frequencies ranging from infrared to dc and including: several amplifiers, a variety of multivibrators, a variable potentiometer, a variety of multiposition switches, an analog-to-digital converter, and a 2-stage cooler. Most, if not all, of these blocks are really integrated circuits, i. e., if one compares the simplified redesigned circuit, rather than the conventional circuit, with the final device, there is a recognizable parts correlation.

Westinghouse makes some of its circuits by dendritic growth of single crystal germanium. The product is a long optically flat ribbon which requires no lapping. Conventional techniques of diffusion, evaporation and plating have been applied to it as it leaves the melt, and, therefore, germanium semiconductor devices have been completed in one operation, except only for attachment of leads. More recently, multi-zoned germanium crystals are being grown as dendrites, thus reducing the number of separate steps to a finished circuit. These circuits have at least three layers of zones and two interfaces. A combination of these two techniques to produce electronic equipment of the order of complexity of amplifiers is a long range objective. In the meantime, investigation of the feasibility of duplicating this work with silicon, and with III-V compounds, is under way in order to improve heat- and radiation-resistance of the products.

Lesk et al (ref 42) have pointed out some rather fundamental limitations to integrated circuits. For example, whereas use of separate component parts permits choice of parts made from a variety of materials in order to obtain superior properties, use of integrated circuits sharply limits such choices and the inevitable result is more limited versatility, wider tolerances, and higher power dissipation. Since major technical problems of production of integrated circuits have not yet been solved, it seems likely that electronic equipment available commercially in the next decade will probably take the form of hybrid structures comprising both individually fabricated parts and single-process parts arrays all mounted or processed onto an insulating substrate. Even when technical problems of production of integrated circuits are solved, it is probable that individually fabricated parts will still be included in cases where optimum performance is required.

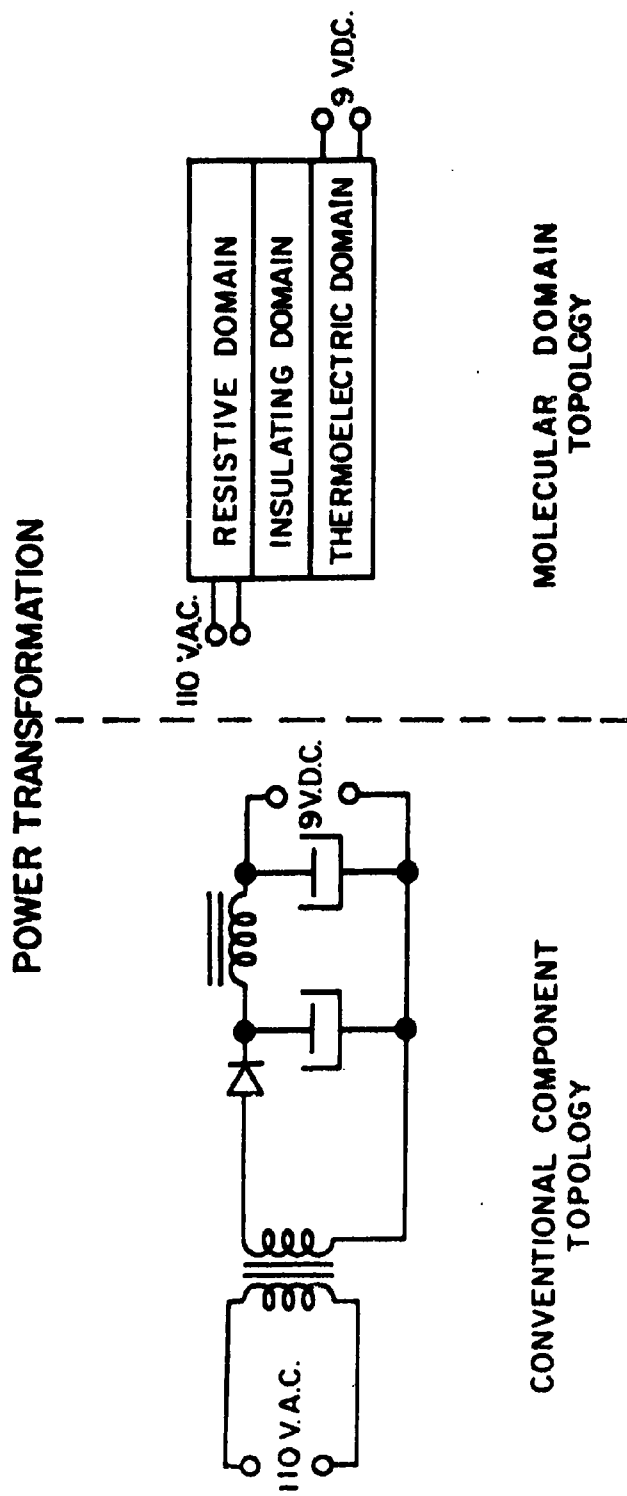


Figure 25. Power transformation by "molecular electronics": Left-hand side, a circuit for a conventional ac-to-dc converter requires a transformer, diode, and filter elements; right-hand side, the functional circuit consists of a 3-domain semiconductor block (Westinghouse Electric Corp.).

5. CONCLUSIONS

A. Industrial practice illustrates the ingenuity of electronic scientists in combining the immediately usable portions of the three major microminiaturization techniques to produce salable circuits. Although it is generally inferred that 2D-type circuits will eventually replace the assembled-part 3D-type of circuit and that integrated circuits will in turn eventually replace 2D-type circuits, circuits of at least the next decade will probably represent hybrid structures. For this reason research and development in all three techniques is necessary in order to combine the best features of each.

B. The first microminiaturization technique discussed, assembly of pretested conventional or specially designed component parts, is already in active commercial use. The second technique, printing or vapor deposition of multi-component assemblies, is in the initial stages of commercial exploitation; although devices with 2D-type passive parts and attached 3D-type active parts are available, realization of full potentialities awaits commercial reduction to practice of 2D-type active parts. The third technique, preparation of complete circuits from a solid block of semiconductor material is also in the initial stages of commercial production; however, since the problems to be overcome prior to wide commercial production are larger than those associated with the second technique, the time scale to production will probably also be larger, but the ultimate benefits should be greater.

C. In the past year, the most significant development in the first discussed technique is that of pelletized parts, in the second technique is most probably that of thin-film tunneling active devices, and in the third technique is possibly the development of laminar layers of controlled conductivity type, resistivity, and thickness.

D. Production problems in the first-discussed technique, disciplined parts geometry excepted, are principally mechanical ones. In the second discussed technique, improved interconnection schemes are still needed and reliability, especially for the thin-metal-film types, has to be established. In the third technique, the relatively new arts of semiconductor processing, and of circuit redesign in terms of desired functions, have to be extended and refined, and such problems as heat dissipation have to be solved.

6. ACKNOWLEDGMENT

The authors wish to thank the following companies for their cooperation and assistance in submitting photographs and/or technical information for this paper: Aerovox Corp., Amphenol-Borg Electronics Corp., Cleveland Metal Specialties Co., Corning Glass Works, General Electric Co., Hamilton Standard Div. United Aircraft Corp., Hughes Aircraft Co., International Resistance Co., Lear, Inc., P. R. Mallory and Co., Inc., Pacific Semiconductors, Inc., Republic Aviation Corp.,

Sprague Electric Co., Servomechanisms, Inc., The Sippican Corp., Sperry Rand Corp., and Texas Instruments, Inc.

Appreciation is also extended to Edith D. Olson for assembling some of the most recent of the references given herein, and to Norman J. Doctor for preparation of Table II.

7. REFERENCES

- (1) Brunetti, C., "A New Venture into Microminiaturization", 1957 IRE National Convention Record, Part 6, March 1957, p. 3.
- (2) Brodzinsky, A., Chairman, "Final Report of ONR Study Group on Microelectronics", ONR-7, Office of Naval Research, Dept. of the Navy, Washington, D. C., June 1960.
- (3) Doctor, N. J. and Davies, E. M., "Microminiature Components for Electronic Circuits," Electrical Manufacturing, 1958, 62, No. 2, pp. 94-97.
- (4) Suran, J. J., "Circuit Considerations Relating to Microelectronics," Proceedings of the IRE, 1961, 49, No. 2, pp. 420-426.
- (5) Hall, E. C. and Jansson, R. M., "3-D Packaging Reduces Size of Electronic Units," Electronics, 1959, 32, No. 41, pp. 62-65.
- (6) Rogers, A. W., "The Micromodule Design Concept in Electronics," Electrical Manufacturing, 1958, 62, No. 1, pp. 46-49.
- (7) Gordon, S. H. and Doctor, N. J., "Miniature Digital Program Timer," Electro-Technology, 1961, 67, No. 2, pp. 142-144.
- (8) Klass, P. J., "Welded Modules Reduce Component Size," Aviation Week, 1959, 71, No. 8, pp. 104-109.
- (9) Bierman, H. and Haavind, R., "Guidelines to Microminiature Design," Electronic Design, 1960, 8, No. 23, pp. 61-98.
- (10) Prugh, T. A., Nall, J. R., and Doctor, N. J., "The DOFL Microelectronics Program," Proceedings of the IRE, 1959, 47, No. 5, pp. 882-894; see also Horsey, E. F. and Shergalis, L. D., Editors, "Microminiaturization of Electronic Assemblies," Hayden Book Co., Inc., 1959, New York, N. Y.
- (11) Cunningham, O. B. and Dale, B. V., "The RCA Micromodule Concept," Field Engineers Electronic Digest, 1958, 6, No. 2, p. 32.
- (12) Mackey, D., "The Micro-Module Program," Proceedings 1960 Electronic Components Conference, May 10-12, 1960, Wash., D. C., p. 51.

- (13) Henry, R. L. and Rosen, H. H. , "Summary of Modular Design of Electronics and Mechanized Production of Electronics," Vol. I, 1953, PB-11275, distributed by U. S. Dept. of Commerce, Business and Defense Services Administration.
- (14) Stuhlbarg, S. M. and Sweany, L. P. , "Microminiature Components and Packaging Techniques," preprint of a paper presented at the 1961 International IRE Convention, March 20, 1961, New York, N. Y.
- (15) "The Application of Dot Components to the Packaging of Communications Equipment," Communication Division, Hughes Aircraft Co. , Brochure R-162, Feb. 3, 1961.
- (16) Franklin, P. J. and Horsey, E. F. , "Materials and Techniques for Microminiaturization, Parts I and II," Electrical Manufacturing, 1960, 65, No. 5, pp. 274-280, and 1960, 65, No. 6, pp. 135-140.
- (17) Yetter, G. R. and Hall, L. L. , "A 2D 30-MC IF Amplifier," TR-894, Diamond Ordnance Fuze Laboratories, 24 February 1961.
- (18) Hastie, E. G. , Diamond Ordnance Fuze Laboratories, unpublished work.
- (19) Krawczyk, J. , Diamond Ordnance Fuze Laboratories, unpublished work.
- (20) Perugini, M. M. and Lindgren, N. , "Microminiaturization," Electronics, 1960, 33, no. 48, pp. 78-108.
- (21) McLean, J. , "New Characteristics Held Mixed Thin Film Possibility," Electronic News, March 6, 1961, 6.
- (22) Bullis, L. H. , Isler, W. E., and Boesman, W. E. , Diamond Ordnance Fuze Laboratories, unpublished work.
- (23) Kinsella, J. J. and Schwertz, F. A. , "2D Etch-Formed RC Circuits," Proceedings 1960 Electronic Components Conference, 1960, pp. 29-32.
- (24) Selvin, G. L. , "The Sylvania Microminiature Module," Proceedings 1960 Electronic Components Conference, 1960, pp. 46-50.
- (25) McLean, D. A. , "Microminiaturization with Refractory Metals," 1959 WESCON Convention Record, Part 6 (1959), pp. 118-121.
- (26) Hebb, E. L. , Diamond Ordnance Fuze Laboratories, unpublished work.

- (27) Belknap, D., "Microlamp," 1959 WESCON Convention Record, Part 6, 1959, pp. 118-121.
- (28) Counihan, R. G., Beatty, H. J., Carroll, W. N., Frye, G. D., Glang, R., Jenny, F. F., Lindsay, R. L., Thun, E. R. and Wajda, E. S., "Thin Film Circuit Functions," Final Report 1 August 1959 to 31 July 1960, Contract No. DA36-039, sc-84547 SCL-21011, IBM, Federal Systems Div., Kingston, New York.
- (29) "Multilayer Semiconductor Deposition," Electronics, 1960, 33, No. 28, pp. 66-67.
- (30) "Titanium Tunnel Diodes," Electronic Design, 1961, 9, No. 5, p. 6.
- (31) Spratt, J. P., Schwarz, R. F. and Kane, W. M., "Hot Electrons in Metal Films: Injection and Collection", Physical Review Letters, 1961, 6, No. 7, pp. 341-342.
- (32) Maguire, T., "Electron Beam Processes," Electronics, 1960, 33, No. 29, pp. 59-63.
- (33) Snyder, P. E., "Chemistry of Thermoelectric Materials," Chemical and Engineering News, 1961, 39, No. 11, pp. 102-112.
- (34) "Rare Earth Thermoelectrics Function at High Temperatures," Chemical and Engineering News, 1961, 39, No. 12, p. 48.
- (35) "Peltier Devices Regulate Temperature," Chemical and Engineering News, 1961, 39, No. 6, p. 51.
- (36) Lathrop, J. W., Lee, R. E. and Phipps, C. H., "Semiconductor Networks for Microelectronics," Electronics, 1960, 33, No. 20, pp. 69-78.
- (37) Allegretti, J. E. and Shombert, D. J., "Laminar Junction Layers - New Concept in Microcircuits," Electronics, 1960, 33, No. 49, pp. 55-57.
- (38) "Solid State BCD-to-Decimal Converter Available at Low Cost," Electronic Design, 1961, 9, No. 6, pp. 64-65.
- (39) Anstead, R. J., Diamond Ordnance Fuze Laboratories, unpublished work.
- (40) Wallmark, J. T., "Design Considerations for Integrated Electronic Devices," Proceedings of the IRE, 1960, 48, No. 3, pp. 298-300.
- (41) "Molecular Electronics," Electronic Industries, 1960, 19, No. 3, pp. 100-103.

(42) Lesk, I. A., Holonyak, N., Aldrich, R. W., Brouillette, J. W., and Ghandi, S. K., "A Categorization of the Solid-State Device Aspects of Microsystems Electronics," Proceedings of the IRE, 1960, 48, No. 11, pp. 1833-1841.

DISTRIBUTION

Office of the Director of Defense Research and Engineering
The Pentagon, Washington 25, D. C.
Attn: Technical Library (rm 3E1065) - 2 copies

Department of the Army
Office of the Chief of Ordnance
The Pentagon, Washington 25, D. C.
Attn: ORDTN (Nuclear and Special Components Br)
Attn: ORDTU (GM Systems Br)
Attn: ORDTB (Research Br)
Attn: ORDTW (Artillery and Vehicle Systems Br)
Attn: ORDTS (Infantry and Aircraft Weapons Systems Br)

Director, Army Research Office
Office of the Chief of Research and Development
Department of the Army
Washington 25, D. C.

Director, Developments
Office of the Chief of Research and Development
Department of the Army
Washington 25, D. C.

Director, Special Weapons
Office of the Chief of Research and Development
Department of the Army
Washington 25, D. C.

Commanding General
U. S. Army Ordnance Missile Command
Redstone Arsenal, Alabama
Attn: ORDXM-R (Asst Chief of Staff for R and D)

Commanding General
Army Ballistic Missile Agency
Redstone Arsenal, Alabama
Attn: ORDAB-DG, Director
Attn: ORDAB-DGI
Attn: ORDAB-DGN, Hugh Taylor
Attn: ORDAB-DGR - Dr. Jasper
Attn: ORDAB-DGN, Mr. Farrier
Attn: Dr. Wilhelm Angele, Guidance Control Laboratory

Commanding General
Army Rocket and Guided Missile Agency
Redstone Arsenal, Alabama
Attn: ORDXR-R, Hugh Camp (R and D Div)

Commanding General
Frankford Arsenal
Philadelphia 37, Pennsylvania
Attn: Reference Librarian

Commanding Officer
Picatinny Arsenal
Dover, New Jersey
Attn: Feltman Research and Engineering Laboratories

Commanding General
Ordnance Weapons Command
Rock Island, Illinois
Attn: Tech Library

Commanding Officer
U. S. Army Signal Research and Development Laboratory
Fort Monmouth, New Jersey
Attn: Electronic Components Research Dept

Commanding Officer
U. S. Army, Office of Ordnance Research
Box CM, Duke Station
Durham, North Carolina

Commanding General
White Sands Missile Range, New Mexico
Attn: Tech Library

Office of the Asst Chief of Staff for Intelligence
The Pentagon, Washington 25, D. C.
Attn: Mail and Records Br

Ordnance Technical Intelligence Agency
Arlington Hall Station
Arlington 12, Virginia

Commanding General
Engineer Research and Development Laboratories
U. S. Army
Fort Belvoir, Virginia
Attn: Tech Documents Center

Commanding General
Ordnance Tank-Auto Command
1501 Beard Street
Detroit 9, Michigan

Commanding Officer
Camp Detrick
Frederick, Maryland

Department of the Navy
Chief of Naval Operations
The Pentagon, Washington 25, D. C.
Attn: Research and Development

Department of the Navy
Washington 25, D. C.
Attn: Chief, Office of Naval Research (Bldg T-3)

Commander
U. S. Naval Ordnance Laboratory
White Oak, Silver Spring 19, Maryland
Attn: Tech Library

Department of the Navy
Bureau of Naval Weapons
Washington 25, D. C.
Attn: DLI-3, Tech Library

Commander
Naval Research Laboratory
Washington 25, D. C.
Attn: Solid-State Electronics Br., S. Paull

Commander
U. S. Naval Ordnance Test Station
China Lake, California
Attn: Tech Library

U. S. Army Liaison Officer
U. S. Naval School
Explosive Ordnance Disposal
Indian Head, Maryland

Commander
U. S. Naval Air Missile Test Center
Point Mugu, California

Headquarters, U. S. Air Force
Washington 25, D. C.

Department of the Air Force
Deputy Chief of Staff for Development
The Pentagon, Washington 25, D. C.
Attn: Director of Research and Development

Commander
Air Research and Development Command
Andrews Air Force Base
Washington 25, D. C.

Commander
Air Materiel Command
Wright-Patterson Air Force Base, Ohio
Attn: LMDN (Aeronautical Systems Center)

Commander
Rome Air Development Center
Griffiss Air Force Base, New York

Air Force Cambridge Research Center
Bedford, Massachusetts
Attn: R. Roberts

Components and Techniques Laboratory
Air Research and Development Center
Bedford, Massachusetts
Attn: E. Czerlinsky

Commander
Air Force Special Weapons Center
Kirtland Air Force Base, New Mexico
Attn: Code SWVSA, L. Stewart

Commander
Armed Services Technical Information Agency
Arlington Hall Station
Arlington 12, Virginia
Attn: TIPDR (10 copies)

Commandant
U. S. Marine Corps
Washington 25, D. C.
Attn: Code A04F

National Aeronautics and Space Administration
1520 H Street, N. W.
Washington 25, D. C.
Attn: Div of Research Information

National Security Agency
Fort George G. Meade, Maryland
Attn: T. A. Prugh

Department of Commerce
Technical Services
Technical Reports Section
Washington 25, D. C.
Attn: Acquisition Section (2 copies)

National Bureau of Standards
Washington 25, D. C.
Attn: Library

Boulder Laboratories
National Bureau of Standards
Boulder, Colorado
Attn: Library

U. S. Atomic Energy Commission
Washington 25, D. C.
Attn: Tech Reports Unit

Director, Advanced Research Projects Agency
Washington 25, D. C.
Attn: Chief, Tech Operation Div

Sandia Corporation
Sandia Base
Albuquerque, New Mexico

Los Alamos Scientific Laboratory
Los Alamos, New Mexico
Attn: R. Watt/J-16

U. S. Atomic Energy Commission
Germantown, Maryland
Attn: Div of Military Applications (DMA)

Texas Instruments, Inc.
Post Office Box 312
Dallas 21, Texas
Attn: Eugene R. McFarland

Mr. E. G. Shower
Sperry Rand Corp.
Semiconductor Division
South Norwalk, Connecticut

Dr. John J. Bohrer
International Resistance Co.
401 North Broad Street
Philadelphia 8, Pennsylvania

Mr. John A. A. Raper
General Electric Company
Electronics Park
Syracuse, New York

Mr. J. C. Sterling, Jr.
Hamilton Standard Division
United Aircraft Corporation
Windsor Locks, Connecticut

Mr. R. F. Redemske
Servomechanisms/Inc.
Research Division
Goleta, California

Mr. L. A. Darling
Lear, Inc.
Solid State Physics Lab.
11916 West Pico Boulevard
Los Angeles 64, California

Mr. R. J. Settzo
Corning Glass Works
Bradford, Pennsylvania

Documentation, Inc.
2521 Connecticut Avenue, N. W.
Washington 8, D. C.

Mr. Bob G. Bender, Head
Microelectronics Dept.
Hughes Products
Post Office Box 278
Newport Beach, California

Mr. C. E. Maiden, Head
Product Development Section
Microelectronics Division
Pacific Semiconductors, Inc.
14520 Aviation Boulevard
Lawndale, California

Mr. Leon Shloss, Asst. Director
Public Relations
Republic Aviation Corp.
Farmingdale, Long Island, New York

Mr. Sidney L. Chertok, Manager
Advertising and Sales Promotion
Sprague Electric Company
North Adams, Massachusetts

Mr. S. M. Stuhlbarg, Manager
Microcomponents Department
P. R. Mallory and Co., Inc.
Indianapolis 6, Indiana

Mr. Peter B. Myers, Staff Scientist
Motorola
Semiconductor Products Division
5005 East McDowell Road
Phoenix, Arizona

Mr. P. C. Cameron
Aerovox Corporation
New Bedford, Massachusetts

Mr. R. P. Thornton, General Manager
Packaged Electronics Division
Amphenol-Borg Electronics Corp.
2801 South 25th Avenue
Broadview, Illinois

Mr. Al Gross, Chief Engineer
Electronics Division
Cleveland Metal Specialties Co.
1783 East 21st Street
Cleveland 14, Ohio

Hinman, W. S., Jr. /McEvoy, R. W.
Apstein, M. /Gerwin, H. L. /Guarino, P. A. /Kalmus, H. P.
Fong, L. B. C. /Schwenk, C. C. /Sures, A. H.
Hardin, C. D., Lab 100
Horton, B. M., Lab 200
Rotkin, I., Lab 300
Tuccinardio, T. E., Lab 400
Hatcher, R. D., Lab 500
Campagna, J. H., Lab 600
White, H. L. /Apolenis, C. J., Div 700
DeMasi, R., Div 800
Franklin, P. J. /900 (5 copies)
Horsey, E. F., Lab 900 (5 Copies)
Seaton, J. W. /260
Technical Reports Unit/800 (3 copies)
Technical Information Office, 010 (10 copies)
DOFL Library (5 copies)
Lilimatainen, T. M. /920
Doctor, N. J. /920 (50 copies)
Williams, D. /920
Kaiser, Q. C. /920
Benderly, A. A. /910
Van Trump, J. H. /930

TWO PAGES OF ABSTRACT CARDS FOLLOW

AD Diamond Ordnance Fuze Laboratories, Washington 25, D. C. STATUS OF MICROMINIATURIZATION -- JUNE 1961 Eleanor F. Horsey and Philip J. Franklin	Accession No.	AD Diamond Ordnance Fuze Laboratories, Washington 25, D. C. STATUS OF MICROMINIATURIZATION -- JUNE 1961 Eleanor F. Horsey and Philip J. Franklin	Accession No.
UNCLASSIFIED 1. Miniature electronic equipment 2. Subminiature electronic equipment 3. Printed circuits-Development	TR-951 1 June 1961 26 pp. text 25 pp. illustrations Dept. of Army Proj. DA-5N06-01-010, OMS 5530.11.56900 DOFL Proj. 90292 UNCLASSIFIED Report The status of microminiaturization is summarized under the following three headings: (1) assembly of pretested conventional or specially designed component parts, (2) printing or vapor deposition of multi-component assemblies on flat insulating substrates, and (3) preparation of complete circuits from a solid block of semiconductor material. Under the first heading, new developments include imitation 2D-type structures, and pelletized parts. Under the second heading, the evolution of the 2D thin-film type of construction into experimental circuits containing all thin-film passive parts is shown. The logical next step, preparation of circuits containing thin-film active as well as passive parts, is discussed. Under the third heading, new developments in integrated and functional circuits are presented. The trend of current work points to the conclusion that equipment available commercially in the next decade will probably take the form of hybrid structures comprising both individually fabricated parts, and single-process parts arrays, all mounted or processed onto an insulating substrate.	UNCLASSIFIED 1. Miniature electronic equipment 2. Subminiature electronic equipment 3. Printed circuits-Development	UNCLASSIFIED 1. Miniature electronic equipment 2. Subminiature electronic equipment 3. Printed circuits-Development
AD Diamond Ordnance Fuze Laboratories, Washington 25, D. C. STATUS OF MICROMINIATURIZATION -- JUNE 1961 Eleanor F. Horsey and Philip J. Franklin	Accession No.	AD Diamond Ordnance Fuze Laboratories, Washington 25, D. C. STATUS OF MICROMINIATURIZATION -- JUNE 1961 Eleanor F. Horsey and Philip J. Franklin	Accession No.
UNCLASSIFIED 1. Miniature electronic equipment 2. Subminiature electronic equipment 3. Printed circuits-Development	TR-951 1 June 1961 26 pp. text 25 pp. illustrations Dept. of Army Proj. DA-5N06-01-010, OMS 5530.11.56900 DOFL Proj. 90292 UNCLASSIFIED Report The status of microminiaturization is summarized under the following three headings: (1) assembly of pretested conventional or specially designed component parts, (2) printing or vapor deposition of multi-component assemblies on flat insulating substrates, and (3) preparation of complete circuits from a solid block of semiconductor material. Under the first heading, new developments include imitation 2D-type structures, and pelletized parts. Under the second heading, the evolution of the 2D thin-film type of construction into experimental circuits containing all thin-film passive parts is shown. The logical next step, preparation of circuits containing thin-film active as well as passive parts, is discussed. Under the third heading, new developments in integrated and functional circuits are presented. The trend of current work points to the conclusion that equipment available commercially in the next decade will probably take the form of hybrid structures comprising both individually fabricated parts, and single-process parts arrays, all mounted or processed onto an insulating substrate.	UNCLASSIFIED 1. Miniature electronic equipment 2. Subminiature electronic equipment 3. Printed circuits-Development	UNCLASSIFIED 1. Miniature electronic equipment 2. Subminiature electronic equipment 3. Printed circuits-Development

REMOVAL OF EACH CARD WILL BE NOTED ON INSIDE BACK COVER, AND REMOVED CARDS WILL BE TREATED AS REQUIRED BY THEIR SOURCE'S CLASSIFICATION.